CORNERSTONE

Design guidelines for the third fabrication call – June 2017

Mask submission deadline – Friday 28th July 2017

1. File format

Designs must be submitted in a Graphical Database System file format (extension *.gdsII*). Ensure a manufacturing grid size of no smaller than 1 nm is used.

We recommend dedicated lithography editing software is used in the design of the *.gdsII* file.

2. Design rules

It is important that designs conform to the following design rules to ensure clarity and correct processing. For this third call, we will process chips with a 500 nm thick silicon core on a 3 µm thick BOX (Buried OXide) layer. We will offer two etch processes: 1) a shallow silicon etching of 160 nm, and 2) a deep silicon etching of 500 nm to the BOX layer. There will be no cladding layer, unless specifically requested upon mask submission.

2.1 Design area

The standard user cell has dimensions of **7 x 7 mm²**. If cleaved facets are required for edge coupling, the total writing area should be reduced to 7 x 6 mm² as an overlay (or bleed) of 500 µm should be included, as shown in Figure 1. Please note that the input/output waveguides should extend into the bleed area.

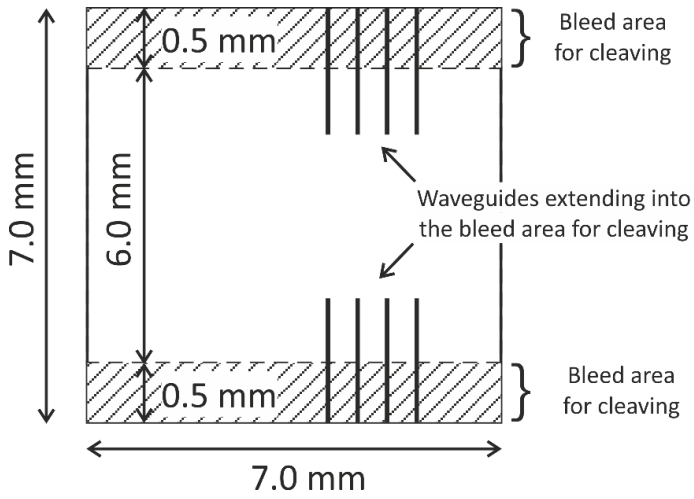


Figure 1 – User cell design area layout.

2.2 GDS layers

Each lithographic step in the fabrication process flow is identified by a specific GDS layer/s. These are as follows:

Silicon Etch 1 (Grating couplers) – GDS Layer 6 (Dark field) – 160 nm

This layer is used to define grating couplers, which are fabricated with 160 nm shallow silicon etching. Positive tone e-beam resist is used, therefore the drawn area is etched.

Silicon Etch 2 (Waveguiding layer) – GDS Layer 3 (Light field) & GDS Layer 4 (Dark field) – 500 nm

This layer defines the waveguides, and is split into two separate GDS layer numbers, patterned into the same resist and etched together:

GDS Layer 3: Drawn objects on this layer will be protected from the silicon etch. Users should draw the waveguides and any other features to remain following etching to the BOX. During fracturing processing for the e-beam, this will be translated into a pattern that defines 5 µm wide trenches on either side of the waveguides drawn in GDS layer 3 (see Figure 2).

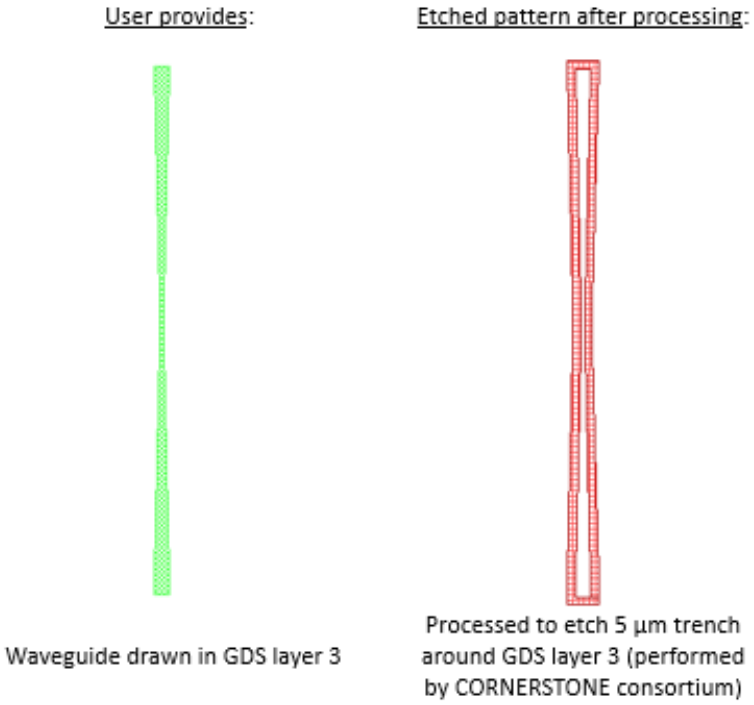


Figure 2 - Description of GDS layer 3 processing.

GDS Layer 4: Drawn objects on this layer will be exposed to the silicon etch to the BOX. This layer is intended for photonic crystal, and similar structures that require small feature sizes (150 nm < feature size < 300 nm). This layer will be written with an e-beam spot size of approximately 5 nm to ensure accurate translation of patterns into the resist. Therefore, the pattern density for this layer should be less than 0.5% of the total design area in order to reduce the e-beam writing time. An example photonic crystal structure is shown in Figure 3. The important thing to note here is that the waveguide layer drawn in GDS layer 3 should overlap the structures drawn in GDS layer 4, so that when the 5 µm trenches are generated by the CORNERSTONE consortium there is a continuous waveguide.

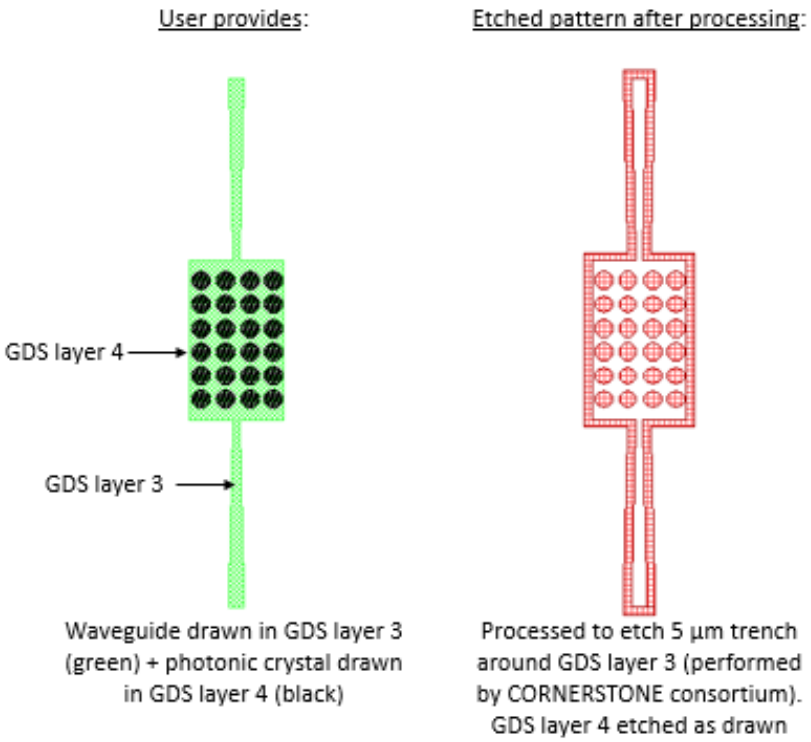


Figure 3 – Example photonic crystal structure using GDS layers 3 & 4.

Cell Outline – GDS Layer 99

This layer defines the design space (7 x 7 mm^2).

Bleed Area – GDS Layer 98

This layer defines the bleed area that will be cleaved if requested by the user. Ensure that waveguides extend fully into this area.

If no cleaving is required, users can fill the entire design space defined in GDS layer 99.

Note: You do not need to add fabrication alignment marks to your design.

2.3 Minimum feature sizes and tolerances

Minimum feature sizes for each GDS layer are detailed in Table 1.

A minimum spacing between waveguides of at least 5 µm is recommended to avoid power coupling.

An overlap of at least 100 nm between GDS layer 6 (Silicon Etch 1 – 160 nm) and GDS layers 3 & 4 (Silicon Etch 2 – 500 nm) is recommended to account for the alignment tolerance between layers.

2.4 Design rules summary

A summary of the design rules and GDS layer numbers described in this section is detailed in Table 1 below.

Table 1 – Design rules summary.

Layer description	GDS number/s	Field	Maximum pattern density	Minimum feature size
Silicon Etch 1 (160 nm)	6	Dark	N/a	150 nm
Silicon Etch 2 (500 nm)	3	Light	N/a	150 nm
	4	Dark	0.5%	
Cell Outline	99	N/a	N/a	N/a
Bleed Area	98	N/a	N/a	N/a

2.5 GDSII template file

A GDSII template file titled 'CORNERSTONE MPW Run 3 GDSII Template' has been made available containing the information described in this section. Ensure that all submitted designs fit within the specified area, and that only the designated GDS layer numbers are used.

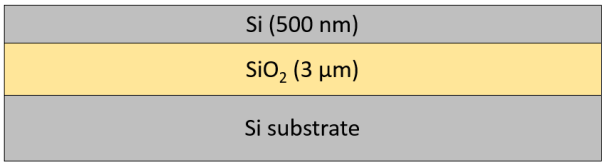
3. Process flow

The patterns will be processed by e-beam lithography on a single-side polished Silicon-on-Insulator (SOI) wafer, with the following nominal parameters:

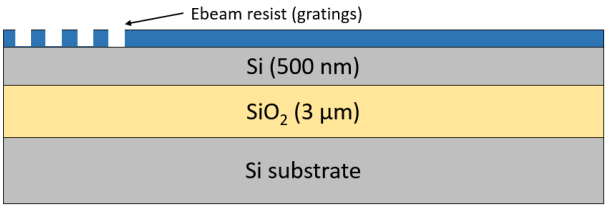
- Crystalline silicon (Si) substrate with a thickness h_{sub} = 675 ± 15 µm
- Thermal silica (SiO_2) BOX layer with a thickness h_{box} = 3 µm
- Crystalline silicon (Si) core layer with a thickness h_{wg} = 500 nm

The schematic description of the process flow is given below:

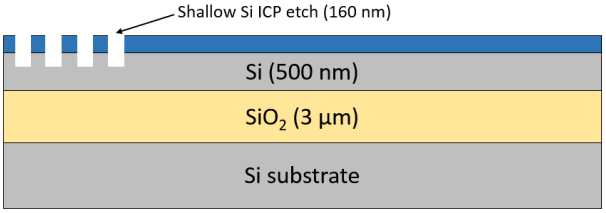
1. Starting SOI substrate



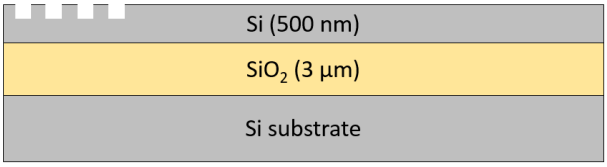
2. E-beam patterning for Silicon Etch 1 (GDS layer 6) – 160 nm etch



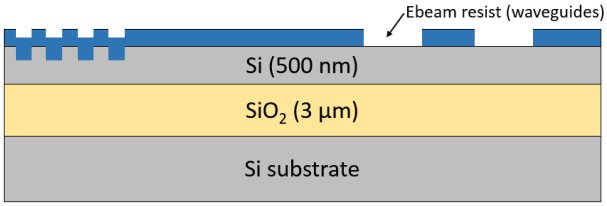
3. Shallow Si ICP etch (160 nm etch depth)



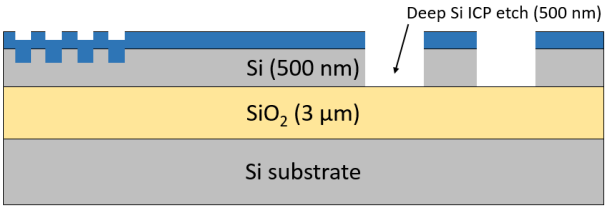
4. E-beam resist strip



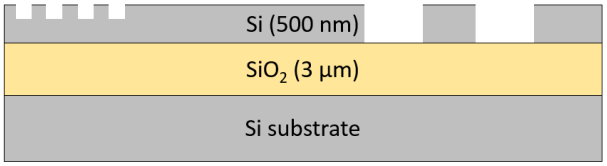
5. E-beam patterning for Silicon Etch 2 (GDS layers 3 & 4) – 500 nm etch



6. Deep Si ICP etch (500 nm etch depth)



7. E-beam resist strip



4. Mask submission procedure

Ensure that the top cell in your GDSII file is titled 'Cell0_*[Name of Institution]*'.

In order to submit your mask design (before Friday 28th July 2017), visit the CORNERSTONE website (www.cornerstone.sotonfab.co.uk) and click on the 'Mask Submission' link at the top of the page. Complete the web-form and click the submit button. You can then expect a link and login details for the mask submission module to be emailed to you within the next 24 hours.

Note: This web-form will not go live until Monday 10th July 2017, after the second call mask submission deadline has passed.

5. Technical support

If you have any questions relating to the fabrication process or design rules, please contact the CORNERSTONE coordinator Dr Callum Littlejohns (cornerstone@soton.ac.uk) or Dr Graham Sharp (graham.sharp@glasgow.ac.uk).

As this is an experimental platform, the CORNERSTONE consortium only offers a standard grating coupler design for 1550 nm wavelength. Please contact cornerstone@soton.ac.uk should you require the GDSII file for this component.

6. Device delivery

A total of 4 cells will be delivered to each user. A tentative delivery date of Friday 29th September 2017 has been set.

7. Feedback

Any feedback is always welcomed, including device performance data, future interests for the CORNERSTONE project etc. Email cornerstone@soton.ac.uk with your comments.