



# CORNERSTONE

## Quick reference design guidelines for the fourteenth fabrication call – June 2019

**Sign-up deadline – Friday 19<sup>th</sup> July 2019**

**Mask submission deadline – Friday 30<sup>th</sup> August 2019**

File format = *.gdsII*.

Manufacturing grid size = 1 nm.

Design area = **11.47 x 4.9 mm<sup>2</sup>** or **5.5 x 4.9 mm<sup>2</sup>**, with 0.5 mm bleed regions on the east and west facets if desired.

Top cell name: 'Cell0\_*[Name of Institution]*'.

### **1. Major changes to design submission process**

All design submissions, even those that are supported by EPSRC funding, must agree with the terms and conditions:

[www.cornerstone.sotonfab.co.uk/terms-and-conditions](http://www.cornerstone.sotonfab.co.uk/terms-and-conditions)

Under no circumstances will we accept designs without agreement with the terms.

Therefore, we strongly recommend that the terms and conditions are pre-authorized by your institution prior to the mask submission date.

Section 7 of the CORNERSTONE 14th Call - Design Rules.pdf document details the design submission process in detail.

### **2. Design rule changes from previous 500 nm SOI platform call (MPW #9)**

The following is a list of design rule changes from the previous 500 nm SOI platform design rules:

1. Minimum feature size for heater filament layer (GDS layer 39) increased to 2  $\mu\text{m}$ .
2. Standard heater design modified.
3. Top SiO<sub>2</sub> cladding layer thickness increased to 2  $\mu\text{m}$ .

### **3. Design rules summary**

A summary of the design rules and GDS layer numbers can be found in Table 1 below.

Table 1 – Design rules summary.

Layer description	GDS number	Field	Min. feature size	Min. gap	Max. feature width	Target critical dimension
Silicon Etch 1 (160 nm ± 15 nm)	6	Dark	200 nm	250 nm	20 µm	280 nm
			200 nm	300 nm	N/a	
Silicon Etch 2 (300 nm ± 20 nm)	3	Light	350 nm	200 nm	N/a	450 nm
	4	Dark	200 nm	350 nm		
Heater Filaments	39	Light	2 µm	10 µm	N/a	2 µm
Heater Contact Pads	41	Light	2 µm	10 µm	N/a	2 µm
Bleed Area	98	N/a	N/a	N/a	N/a	N/a
Cell Outline	99	N/a	N/a	N/a	N/a	N/a
Labels*	100	Dark	250 nm	250 nm	N/a	N/a

\*Features drawn in the Labels layer will be merged into Silicon Etch 2 by the CORNERSTONE team.

#### 4. Minimum feature sizes, tolerances and other design rules

- Minimum feature sizes, minimum gaps, and maximum feature widths for each GDS layer are detailed in Table 1.
- The target critical dimension for each GDS layer is listed in Table 1. Note that other feature sizes may have a small dimensional bias.
- A minimum spacing between waveguides of at least 5 µm is recommended to avoid power coupling.
- An overlap of at least 200 nm between GDS layers is essential to account for the alignment tolerance between layers.
- All structures drawn in GDS layer 6 (Grating couplers) must overlap by at least 200 nm with GDS layer 3 (Waveguides).
- An overlap of at least 10 µm between GDS layer 39 (Heater Filaments) and GDS layer 41 (Heater Contact Pads) is recommended for optimal heater performance.
- Ensure all structures drawn in GDS layer 6 (Grating couplers) do not overlap with either GDS layer 39 (Heater Filaments) or GDS 41 (Heater Contact Pads).

#### 5. Technical support

For all queries, email [cornerstone@soton.ac.uk](mailto:cornerstone@soton.ac.uk).