Engineering and Physical Sciences Research Council

CORNERSTONE

Design guidelines for the seventeenth fabrication call – December 2019

Sign-up deadline – Friday 17th January 2020

Mask submission deadline – Friday 6th March 2020

File format = *.gdsII*.

Manufacturing grid size = 1 nm.

Design area = **11.47 x 4.9 mm^2** or **5.5 x 4.9 mm^2**, with 0.5 mm bleed regions on the east and west facets if desired.

Top cell name: 'Cell0_*[Name of Institution]*'.

1. Terms & conditions and cost

All design submissions must agree with the terms and conditions:

www.cornerstone.sotonfab.co.uk/terms-and-conditions

Under no circumstances will we accept designs without agreement with the terms.

Therefore, we strongly recommend that the terms and conditions are pre-authorised by your institution prior to the mask submission date.

A purchase order (PO) must be uploaded at the same time as submitting your mask design in order pay the access fee, detailed in Table 1 below. Purchase orders will not be accepted via email.

Table 1 – Access cost.

Design Area	Access Cost*
11.47 x 4.9 mm^2	£35,000
5.5 x 4.9 mm^2	£20,000

*Quoted prices are exclusive of VAT, import duties, withholding taxes etc.

For information about setting up CORNERSTONE as a supplier to your institution, please contact cornerstone@soton.ac.uk.

Section 7 of the CORNERSTONE 17th Call - Design Rules.pdf document details the design submission process in detail.

2. Design rule changes from previous 220 nm SOI platform active device call (MPW #11)

The following is a list of design rule changes from the previous 220 nm SOI platform active device design rules (MPW #11):

1. Minimum gap in the electrode layer (GDS layer 13) reduced to 2 µm.
2. Additional mask processing steps performed by CORNERSTONE introduced to ensure compliance with design rules (see Section 8 of "CORNERSTONE 17th Call - Design Rules.pdf").
3.

3. Design rules summary

A summary of the design rules and GDS layer numbers can be found in Table 2 below.

Table 2 – Design rules summary.

Layer description	GDS number	Field	Min. feature size	Min. gap	Max. feature width	Target critical dimension
Silicon Etch 1 (70 nm ± 10 nm)	6	Dark	200 nm	250 nm	20 µm	315 nm
			200 nm	300 nm	N/a	
Silicon Etch 2 (120 nm ± 10 nm)	3	Light	350 nm	200 nm	N/a	450 nm
	4	Dark	200 nm	350 nm		
Silicon Etch 3 (100 nm to BOX)	5	Light	250 nm	250 nm	N/a	250 nm
Low Dose *p*-type Implant	7	Dark	500 nm	500 nm	40 µm	500 nm
Low Dose *n*-type Implant*	8	Dark	500 nm	500 nm	10 µm	500 nm
High Dose *p*-type Implant	9	Dark	500 nm	500 nm	10 µm	500 nm
High Dose *n*-type Implant	11	Dark	500 nm	500 nm	10 µm	500 nm
Vias	12	Dark	3 µm	5 µm	10 µm	5 µm
Electrodes	13	Light	6 µm	2 µm	N/a	2 µm
Bleed Area	98	N/a	N/a	N/a	N/a	N/a
Cell Outline	99	N/a	N/a	N/a	N/a	N/a
Labels**	100	Dark	250 nm	250 nm	N/a	N/a

*Angled implant from the south direction.

**Features drawn in the Labels layer will be merged into Silicon Etch 2 by the CORNERSTONE team.

4. Minimum feature sizes, tolerances and other design rules

- Minimum feature sizes, minimum gaps, and maximum feature widths for each GDS layer are detailed in Table 2.
- The target critical dimension for each GDS layer is listed in Table 2. Note that other feature sizes may have a small dimension bias.
- A minimum spacing between waveguides of at least 5 µm is recommended to avoid power coupling.
- An overlap of at least 200 nm between GDS layers is essential to account for the alignment tolerance between layers.
- All structures drawn in GDS layer 6 (Grating couplers) must overlap by at least 200 nm with GDS layer 3 (Waveguides).
- All structures drawn in GDS layer 5 (Rib protect) should extend 10 µm beyond the edge of GDS layer 3 (Waveguides), with the exception of rib-to-strip transitions.
- All structures drawn in GDS layer 9 and GDS layer 11 (high dose implant layers) should not overlap with GDS layer 3 (Waveguides). The high dose implants will be masked by the hard mask regardless.
- All structures drawn in GDS layer 12 (Vias) must be inclusive of either GDS layer 9 (High Dose *p*-type Implant) or GDS layer 11 (High Dose *n*-type Implant) by at least 500 nm (i.e. the high dose implant layer must extend in all directions at least 500 nm beyond the vias layer).
- All structures drawn in GDS layer 12 (Vias) must be inclusive of the metal contacts drawn in GDS layer 13 (Electrodes) by at least 500 nm (i.e. the electrode layer must extend in all directions at least 500 nm beyond the vias layer).
- Ensure all structures drawn in GDS layer 6 (Grating couplers) do not overlap with either GDS layer 12 (Vias) or GDS 13 (Electrodes).

5. Process parameters overview

A cross-section of a carrier depletion modulator structure is shown in Figure 1, along with the important device parameters, including doping concentrations, listed in Table 3.

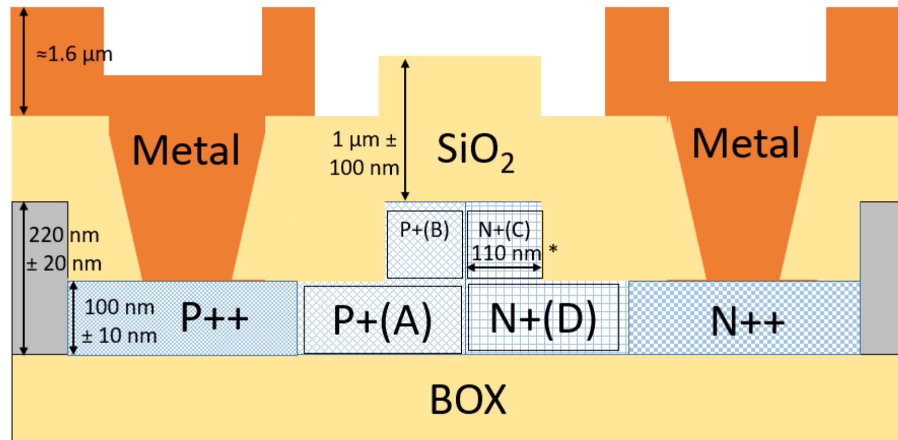

*Figure 1 – Process parameters overview. *The N+ implant is performed at 45°, so the implanted region is fixed at 110 nm from waveguide edge (controlled by the angled implant energy).*

Table 3 – Important device parameters.

Property	Specification
Si overlayer thickness	220 nm ± 20 nm
Grating etch depth	70 nm ± 10 nm
Rib waveguide etch depth	120 nm ± 10 nm
P+ region (A)	≈ 3.8E17 cm^{-3}
P+ region (B)	≈ 1.5E17 cm^{-3}
N+ region (C)*	≈ 7.5E17 cm^{-3}
N+ region (D)*	≈ 1.1E18 cm^{-3}
P++	≈ 1E20 cm^{-3}
N++	≈ 1E20 cm^{-3}
Top cladding SiO_2 thickness	1 µm ± 100 nm
Metal thickness	≈ 1.6 µm

**Note:* The low dose *n*-type implant concentrations are compensated by the background low dose *p*-type implant (i.e. the low dose *n*-type region must fully overlap with the low dose p-type region; otherwise, the actual *n*-type concentrations will be higher than specified).

6. Technical support

For all queries, email cornerstone@soton.ac.uk.