Engineering and Physical Sciences Research Council

CORNERSTONE

Design guidelines for the eighteenth fabrication call – December 2019

Sign-up deadline – Friday 17th January 2020

Mask submission deadline – Friday 6th March 2020

1 Terms & conditions and cost

All design submissions must agree with the terms and conditions:

www.cornerstone.sotonfab.co.uk/terms-and-conditions

Under no circumstances will we accept designs without agreement with the terms.

Therefore, we strongly recommend that the terms and conditions are pre-authorised by your institution prior to the mask submission date.

A purchase order (PO) must be uploaded at the same time as submitting your mask design in order pay the access fee, detailed in Table 1 below. Purchase orders will not be accepted via email.

Table 1 – Access cost.

Design Area	Access Cost*
11.47 x 4.9 mm^2	£10,000
5.5 x 4.9 mm^2	£7,000

*Quoted prices are exclusive of VAT, import duties, withholding taxes etc.

For information about setting up CORNERSTONE as a supplier to your institution, please contact cornerstone@soton.ac.uk.

Section 7 details the design submission process in more detail.

2 Design rule changes from previous 220 nm SOI platform call (MPW #15)

There are no design rule changes from the previous 220 nm SOI platform design rules.

3 IPKISS process design kit

For the greatest functionality, we recommend that you use Luceda's IPKISS software to access the process design kit (PDK), after purchasing the required license. The PDK can be used in either IPKISS.eda (integrated with Mentor Graphics Tanner L-Edit) or IPKISS.flow (stand-alone python scripting).

To obtain a copy of the software and a license key, please contact Luceda by sending an email to info@lucedaphotonics.com, specifying that you require a license for CORNERSTONE PDK usage. Luceda will contact you within 1-2 working days following the receipt of your request to provide a quote for the license. Of course, if you already have a valid license, the PDK can be accessed free of charge.

For more information about Luceda's software offering, please visit www.lucedaphotonics.com.

Once you have access to the Luceda software, in order to obtain a copy of the CORNERSTONE PDK, please contact Luceda support at info@lucedaphotonics.com. An account will be created for you at support.lucedaphotonics.com for any technical support on Luceda's IPKISS software or the CORNERSTONE PDK implementation.

We also have a PDK available for download in GDSII format.

4 Process flow

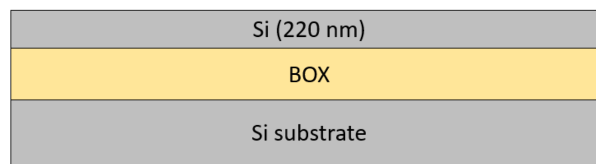
For this eighteenth call, the patterns will be processed on a single-side polished Silicon-on-Insulator (SOI) wafer, with the following nominal parameters:

- Crystalline silicon (Si) substrate
- Thermal silica (SiO_2) Buried OXide (BOX) layer with a thickness h_{box} = 2 µm
- Crystalline silicon (Si) core layer (100)-oriented with a thickness h_{wg} = 220 nm ± 20 nm

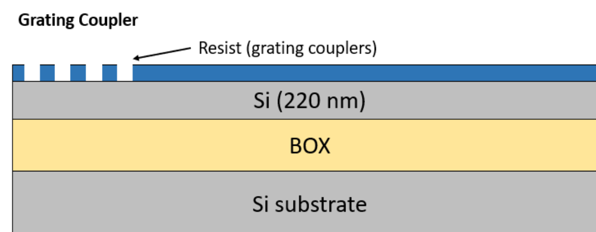
We will offer two silicon etch processes: 1) a shallow silicon etch of 70 nm ± 10 nm, and 2) a full silicon etch to the BOX layer. We will offer a 1 µm ± 100 nm thick silicon dioxide top cladding layer with two metal layers for heaters: 1) heater filaments, and 2) heater contact pads.

The schematic description of the process flow is given below:

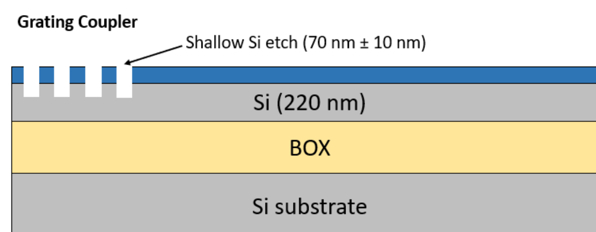
1. Starting SOI substrate



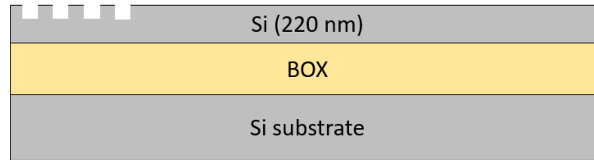
2. Resist patterning for Silicon Etch 1 (GDS layer 6) – 70 nm ± 10 nm etch



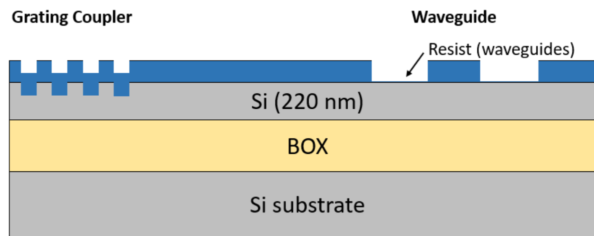
3. Shallow Si etch (70 nm ± 10 nm etch depth)



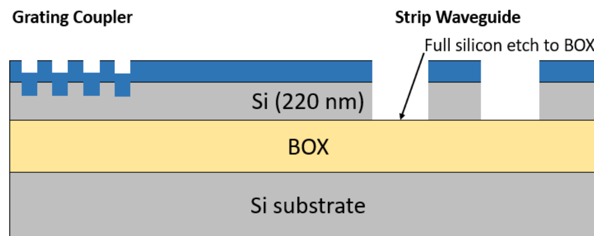
4. Resist strip



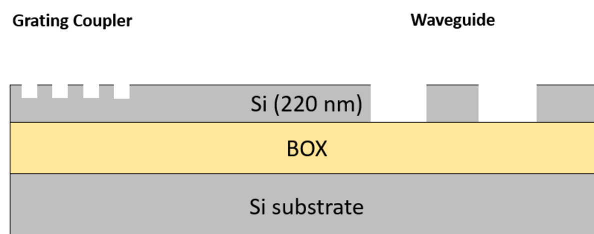
5. Resist patterning for Silicon Etch 2 (GDS layers 3, 4 & 100) – 220 nm full etch to BOX



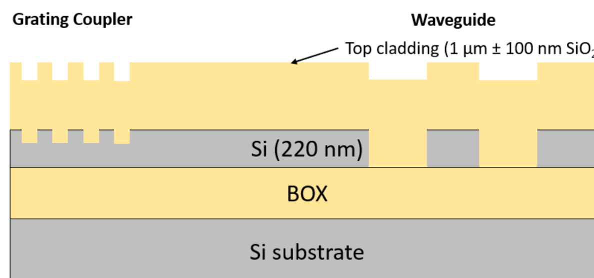
6. Full Si etch (220 nm to BOX)



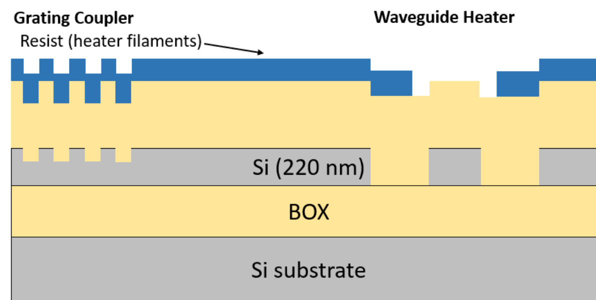
7. Resist strip



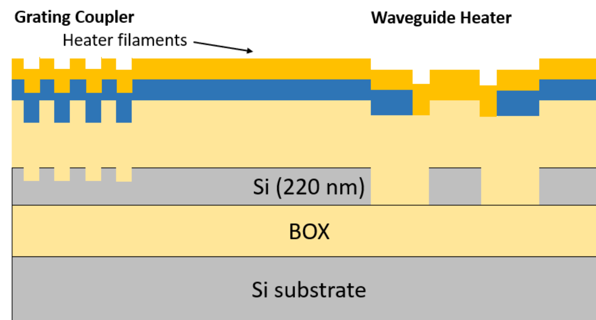
8. Deposition of 1 µm ± 100 nm thick SiO_2 top cladding



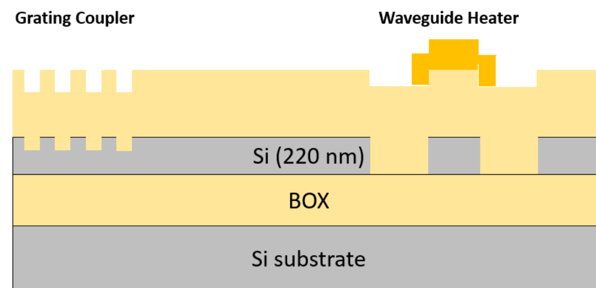
9. Resist patterning for Heater Filaments (GDS layer 39)



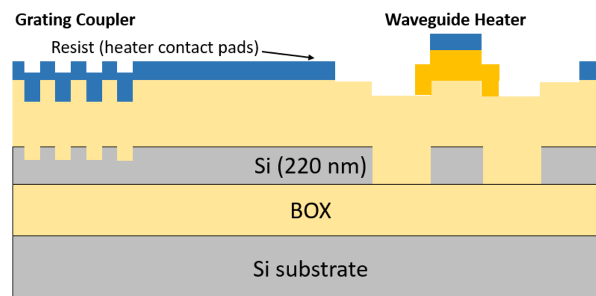
10. Heater filament deposition



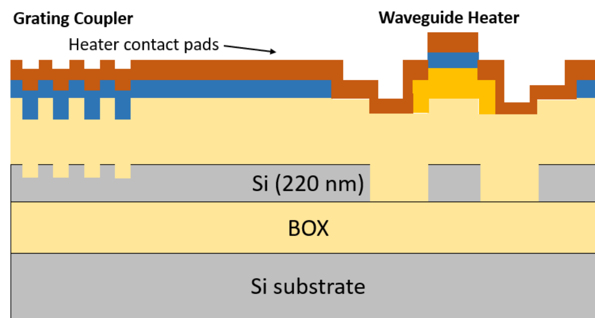
11. Metal lift-off



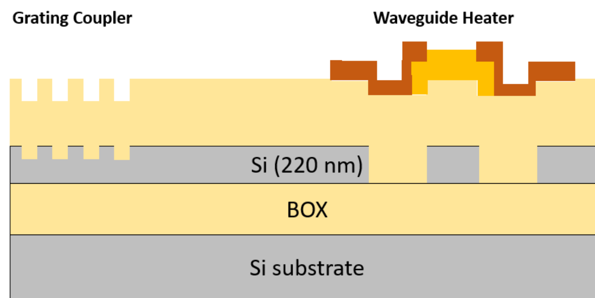
12. Resist patterning for Heater Contact Pads (GDS layer 41)



13. Heater contact pads deposition



14. Metal lift-off



If you require any alternative processing steps (e.g. custom etch depths), we may be able to perform them for a small charge. Email cornerstone@soton.ac.uk with your request.

5 Design rules

It is important that designs conform to the following design rules to ensure clarity and correct processing.

5.1 Design area

The standard user cell has dimensions of **11.47 x 4.9 mm^2**. If cleaved facets are required for edge coupling, the total design area should be reduced to **10.47 x 4.9 mm^2** as an overlay (or bleed) of 500 µm should be included on the east and west facets, as shown in Figure 1a. Alternatively, a smaller cell with dimensions of **5.5 x 4.9 mm^2** may be used. Likewise, if cleaved facets are required for edge coupling, the total design area should be reduced to **4.5 x 4.9 mm^2** as an overlay (or bleed) of 500 µm should be included on the east and west facets, as shown in Figure 1b. Please note that the input/output waveguides should extend fully into the bleed area. If you would like your chips to be cleaved, please indicate this on the submission form when submitting your mask design.

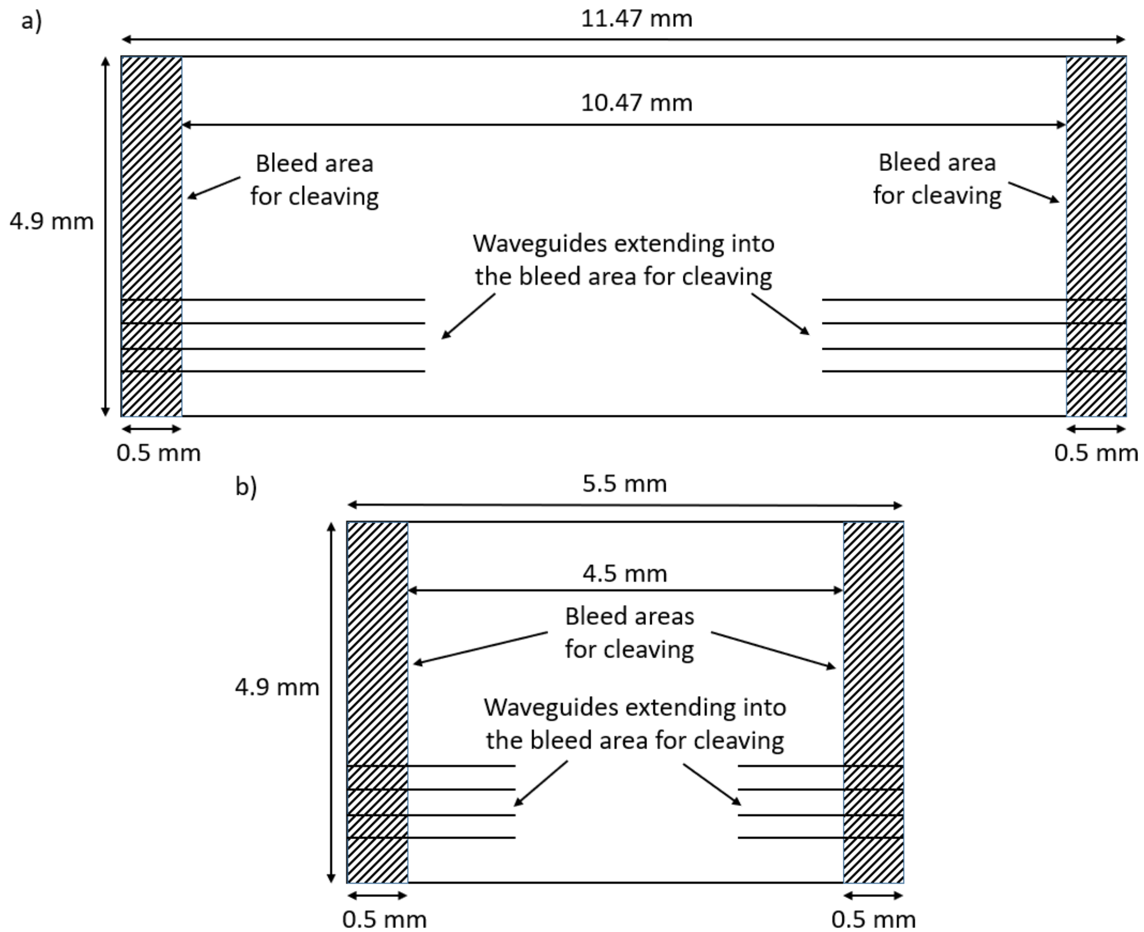


Figure 1 – User cell design area layout for a) 11.47 x 4.9 mm^2, and b) 5.5 x 4.9 mm^2.

5.2 GDS layers

Each lithographic step in the fabrication process flow is identified by a specific GDS layer/s. These are as follows:

Silicon Etch 1 (Grating couplers) – GDS Layer 6 (Dark field) – etch depth: 70 nm ± 10 nm

This layer is used to define grating couplers, which are fabricated with 70 nm shallow silicon etching. The drawn area is etched.

Silicon Etch 2 (Waveguide layer) – GDS Layer 3 (Light field) & GDS Layer 4 (Dark field) – etch depth: 220 nm to BOX

This layer defines strip waveguides and is split into two separate GDS layer numbers, patterned into the same resist and etched together:

> *GDS Layer 3*: Drawn objects on this layer will be protected from the silicon etch. Users should draw the waveguides and any other features to remain following silicon etching. During fracturing processing, this will be translated into a pattern that defines 5 µm wide trenches on either side of the waveguides drawn in GDS layer 3 (see Figure 2).

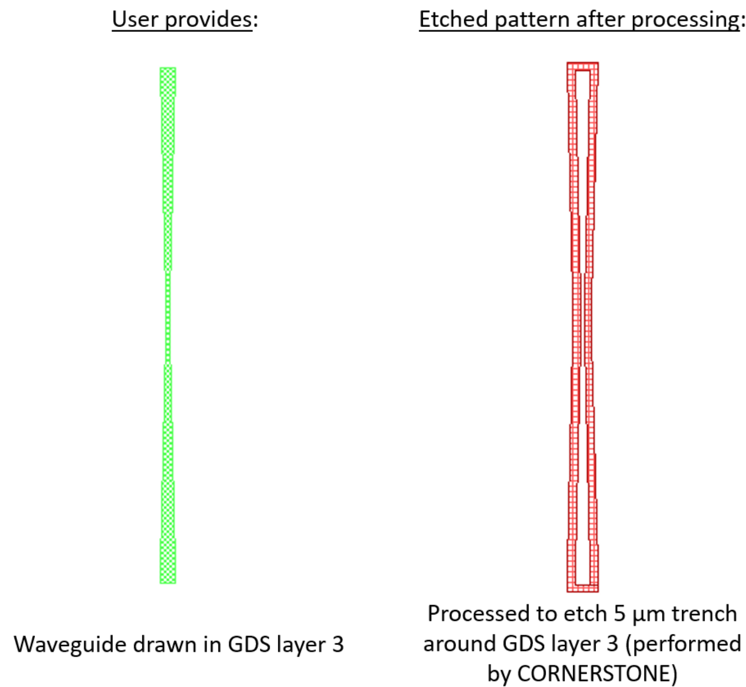


Figure 2 - Description of GDS Layer 3 processing.

GDS Layer 4: Drawn objects on this layer will be exposed to silicon etch. An example photonic crystal structure is shown in Figure 3. The important thing to note here is that the waveguide layer drawn in GDS layer 3 should overlap the structures drawn in GDS layer 4, so that when the 5 µm trenches are generated by CORNERSTONE, a continuous waveguide remains.

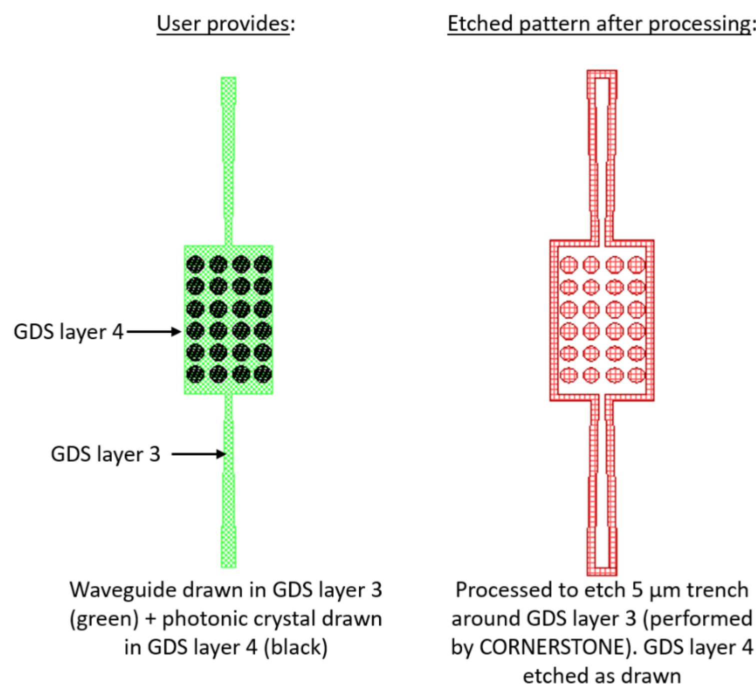


Figure 3 – Example photonic crystal structure using GDS Layers 3 & 4.

Heater Filaments – GDS Layer 39 (Light field)

This layer defines the heater filaments. Drawn objects on this layer will remain after metal lift-off. It is recommended to use a filament width of 2 µm for the best compromise between heater power efficiency and phase tunability.

Heater Contact Pads – GDS Layer 41 (Light field)

This layer defines the heater contact pads. Drawn objects on this layer will remain after metal lift-off.

An example heater layout for a straight waveguide is included in the *.gdsII* template file. The contact pads can be modified according to your probe design.

Bleed Area – GDS Layer 98

This layer defines the bleed area that will be cleaved if requested by the user. Ensure that waveguides that require cleaving extend fully into this area.

If no cleaving is required, users can fill the entire design space defined in GDS layer 99.

Cell Outline – GDS Layer 99

This layer defines the design space boundaries (11.47 x 4.9 mm^2 or 5.5 x 4.9 mm^2).

Labels – GDS Layer 100

This layer defines text labels, which will be merged with Silicon Etch 2 (Waveguides) by the CORNERSTONE team. This layer will not have any design rule checking (DRC) performed.

Note: You do not need to add fabrication alignment marks to your design. Layer-to-layer alignment marks will be added by the CORNERSTONE team, placed outside the design area.

5.3 Minimum feature sizes, target critical dimensions and other design rules

- Minimum feature sizes, minimum gaps, and maximum feature widths for each GDS layer are detailed in Table 2.
- The target critical dimension for each GDS layer is listed in Table 2. Note that other feature sizes may have a small dimensional bias.
- A minimum spacing between waveguides of at least 5 µm is recommended to avoid power coupling.
- An overlap of at least 200 nm between GDS layers is essential to account for the alignment tolerance between layers.
- All structures drawn in GDS layer 6 (Grating couplers) must overlap by at least 200 nm with GDS layer 3 (Waveguides).
- An overlap of at least 10 µm between GDS layer 39 (Heater Filaments) and GDS layer 41 (Heater Contact Pads) is recommended for optimal heater performance.
- Ensure all structures drawn in GDS layer 6 (Grating couplers) do not overlap with either GDS layer 39 (Heater Filaments) or GDS 41 (Heater Contact Pads).

5.4 Design rules summary

A summary of the design rules and GDS layer numbers described in this section is detailed in Table 2 below.

Table 2 – Design rules summary.

Layer description	GDS number	Field	Min. feature size	Min. gap	Max. feature width	Target critical dimension
Silicon Etch 1 (70 nm ± 10 nm)	6	Dark	200 nm	250 nm	20 µm	315 nm
			200 nm	300 nm	N/a	
Silicon Etch 2 (220 nm to BOX)	3	Light	350 nm	200 nm	N/a	450 nm
	4	Dark	200 nm	350 nm		
Heater Filaments	39	Light	2 µm	10 µm	N/a	2 µm
Heater Contact Pads	41	Light	2 µm	10 µm	N/a	2 µm
Bleed Area	98	N/a	N/a	N/a	N/a	N/a
Cell Outline	99	N/a	N/a	N/a	N/a	N/a
Labels*	100	Dark	250 nm	250 nm	N/a	N/a

*Features drawn in the Labels layer will be merged into Silicon Etch 2 by the CORNERSTONE team.

In order to help you ensure that you comply with the design rules, you can also download a design rule check (DRC) checklist from our website and if you have access to Tanner L-Edit software, a .tdb version of the template containing a DRC file that you can run to automatically find any design rule violations (note that the automatic DRC will not check all of the design rules, so it remains very important to read the design rules in detail).

5.5 File format

Designs must be submitted in a Graphical Database System file format (extension *.gdsII*). Ensure a manufacturing grid size of 1 nm is used, as per the 'CORNERSTONE MPW Run 18 GDSII Template' file.

We recommend dedicated lithography editing software be used in the design of the *.gdsII* file.

5.6 GDSII template file

A *.gdsII* template file titled 'CORNERSTONE MPW Run 18 GDSII Template' has been made available containing the information described in this section. Ensure that all submitted designs fit within the specified area, and that only the designated GDS layer numbers are used.

6 Quality assessment

This fabrication run will be qualified by characterising a standard test pattern that is included on the chip (not part of the user cell). The test structures that will be checked after fabrication are reported in Table 3 below, together with the values that are targeted by the CORNERSTONE platform.

Table 3 – Quality assessment parameters.

Test structure	Parameter	Value
Straight single mode waveguide	Propagation loss	< 4 dB/cm for TE mode
MZI integrated 200 µm length heater	Phase shift efficiency	< 30 mW/π phase shift

7 Mask submission procedure

In order to be eligible to submit a design you must first sign-up to this call using the online form found using the link below. This is in order to enable us to prepare the necessary paperwork and plan the fabrication process effectively. The sign-up deadline is **Friday 17th January 2020**.

www.cornerstone.sotonfab.co.uk/work-with-us/sign-up-form

Under no circumstances will we accept any design submissions for which we have not received a sign-up form.

After completing the sign-up form, when you are ready to submit your mask design on or before **Friday 6th March 2020**, follow the link below to the CORNERSTONE website mask submission page:

www.cornerstone.sotonfab.co.uk/work-with-us/mask-submission-form

A purchase order (PO) must be uploaded to this form to pay the access fee. Purchase orders will not be accepted via email.

After completion of the mask submission form, within 24 hours you will be emailed a username and password for the online mask uploading module:

https://www.csfm.cornerstone.sotonfab.co.uk/login

Upload your *.gdsII* file to the CORNERSTONE MPW Run 18 folder, from where the CORNERSTONE team will be able to access it. Ensure that the top cell in your *.gdsII* file is titled 'Cell0_*[Name of Institution]*'.

Note: Other CORNERSTONE users will not be able to view your uploaded files.

For information about setting up CORNERSTONE as a supplier to your institution, please contact cornerstone@soton.ac.uk.

8 Mask processing performed by CORNERSTONE

Upon receipt of your *.gdsII* file, the CORNERSTONE team will perform the following mask processing steps in order to produce the final mask, based on the descriptions provided in Section 5.2:

Silicon Etch 2 (Waveguide layer) – GDS Layer 3 (Light field) & GDS Layer 4 (Dark field) – etch depth: 220 nm to BOX:

1. Grow Waveguide layer (GDS layer 3) by 5 µm in all directions (grow by 10 µm in the bleed region – GDS layer 98).
2. Subtract the Waveguide layer (GDS layer 3) from the output of (1) to produce the etch trenches around the drawn waveguides.
3. Merge the output of (2) with the dark field Waveguide Etch layer (GDS layer 4) and the Labels layer (GDS layer 100).

9 Technical support

If you have any questions relating to the fabrication process or design rules, please contact the CORNERSTONE co-ordinator Dr Callum Littlejohns (cornerstone@soton.ac.uk).

CORNERSTONE

Engineering and Physical Sciences Research Council

10 Device delivery

A total of 10 replica cells will be delivered to each user. A tentative delivery date of Friday 26th June 2020 has been set.

11 Feedback

Feedback is essential to the CORNERSTONE team. It is required to ensure a continuous improvement to the quality of our services. It is also evidence on the user satisfaction, and a measure to what extent we were able to meet user requirements. Therefore, we kindly ask our users to provide feedback to us, including device performance data, SEM images, future interests for the CORNERSTONE project etc. A feedback form will be sent to you along with your chips.

Alternatively, email cornerstone@soton.ac.uk with your comments.

12 Publication

Please include CORNERSTONE in the acknowledgments section of any publications that result from the chips you receive from CORNERSTONE.