CORNERSTONE

Design guidelines for suspended Si MPW #1 – November 2021

Sign-up deadline – Friday 28th January 2022

Mask submission deadline – Friday 25th February 2022

1 Terms & conditions and cost

All design submissions must agree with the terms and conditions:

www.cornerstone.sotonfab.co.uk/terms-and-conditions

Under no circumstances will we accept designs without agreement with the terms.

Therefore, we strongly recommend that the terms and conditions are pre-authorised by your institution prior to the mask submission date.

If you are from a UK University, there will be no access charge as your chips will be supplied under the EPSRC CORNERSTONE 2 funding. However, you must still agree to the terms and conditions. We are grateful to Compugraphics (https://www.compugraphics-photomasks.com/) who are supporting the CORNERSTONE 2 project with discounted reticles/masks.

A purchase order (PO) must be uploaded at the same time as submitting your mask design in order pay the access fee, detailed in Table 1 below. Purchase orders will not be accepted via email.

Table 1 – Access cost.

Design Area	Access Cost*
11.47 x 4.9 mm^2	£5,200
5.5 x 4.9 mm^2	£3,750

*Quoted prices are exclusive of VAT, import duties/customs fees, withholding taxes etc.

For information about setting up CORNERSTONE as a supplier to your institution, please contact cornerstone@soton.ac.uk.

Section 6 details the design submission process in more detail.

2 IPKISS process design kit

For the greatest functionality, we recommend that you use Luceda's IPKISS software to access the process design kit (PDK), after purchasing the required license. The PDK can be used in either IPKISS.eda (integrated with Mentor Graphics Tanner L-Edit) or IPKISS.flow (stand-alone python scripting).

To obtain a copy of the software and a license key, please contact Luceda by sending an email to info@lucedaphotonics.com, specifying that you require a license for CORNERSTONE PDK usage. Luceda will contact you within 1-2 working days following the receipt of your request to provide a quote for the license. Of course, if you already have a valid license, the PDK can be accessed free of charge.

For more information about Luceda's software offering, please visit www.lucedaphotonics.com.

Once you have access to the Luceda software, in order to obtain a copy of the CORNERSTONE PDK, please contact Luceda support at info@lucedaphotonics.com. An account will be created for you at support.lucedaphotonics.com for any technical support on Luceda's IPKISS software or the CORNERSTONE PDK implementation.

We also have a PDK available for download in GDSII format.

3 Process flow

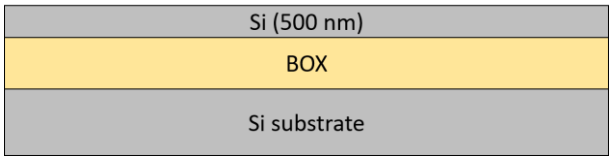
For this call, the patterns will be processed on a single-side polished Silicon-on-Insulator (SOI) wafer, with the following nominal parameters:

- Crystalline silicon (Si) substrate
- Thermal silica (SiO_2) Buried OXide (BOX) layer with a thickness h_{box} = 3 µm
- Crystalline silicon (Si) core layer (100)-oriented with a thickness h_{wg} = 500 nm ± 15 nm

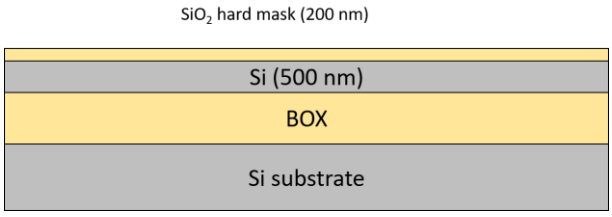
We will offer one silicon etch process: 1) a full silicon etch of 500 nm to the BOX layer, followed by wet HF etching of the BOX layer.

The schematic description of the process flow is given below:

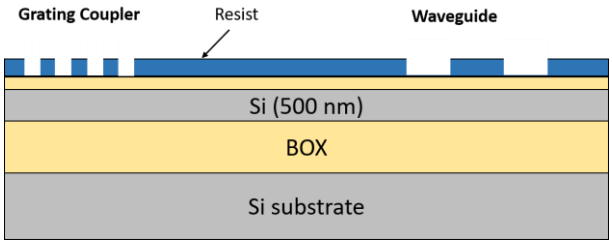
1. Starting SOI substrate



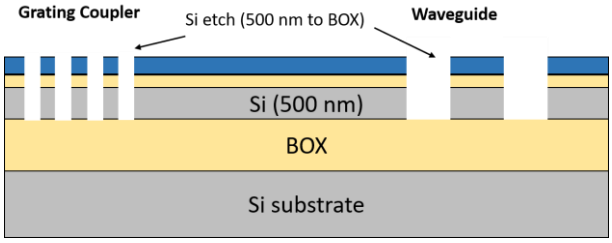
2. Hard mask (SiO_2) deposition – 200nm



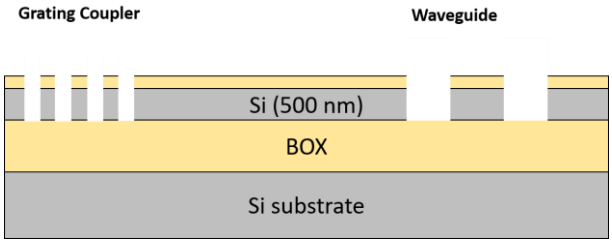
3. Resist patterning for grating couplers and waveguides – GDS layer 404



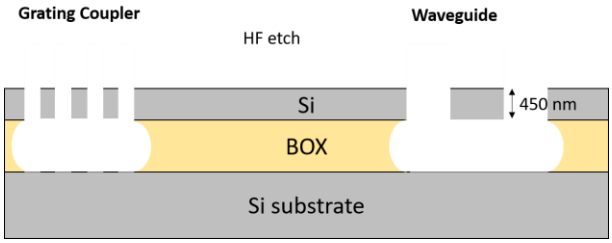
4. Hard mask etch followed by Silicon etch



5. Resist strip



6. HF etch



During this HF etching step, the BOX is undercut by approximately 8 µm in each direction.

If you require any alternative processing steps (e.g. custom etch depths), we may be able to perform them for a small charge. Email cornerstone@soton.ac.uk with your request.

4 Design rules

It is important that designs conform to the following design rules to ensure correct processing. Please note that after HF undercut etching, the thickness of the silicon layer reduces to 450 nm ± 20 nm and the lateral feature size reduces by approximately 70 nm. For example, a silicon feature width of 220 nm after processing in HF reduces to 150 nm. Furthermore, the BOX is undercut by approximately 8 µm in each direction.

Users have the option to either pre-bias or not bias their design. If un-biased, the CORNERSTONE team will perform a 35 nm shrinking of all Si etched features to offset the expected etched feature size growth during HF etching. Note that the -35 nm bias is in all directions, so an etched feature becomes 70 nm narrower. Please notify the CORNERSTONE team to either BIAS/UNBIAS your designs while submitting through the online submission process outlined in Section 6.

4.1 Design area

The standard user cell has dimensions of **11.47 x 4.9 mm^2**. You can also use cell dimensions of **5.5 x 4.9 mm^2**.

4.2 GDS layers

Each lithographic step in the fabrication process flow is identified by a specific GDS layer/s. These are as follows:

Silicon Etch 1 (Grating couplers and waveguide) – GDS Layer 404 (Dark field) – etch depth: 500 nm to the BOX layer

This layer is used to define grating couplers and waveguides, which are fabricated with 500 nm silicon etching.

For users who choose to ask CORNERSTONE **'NOT TO BIAS'**: The drawn area is etched.

For users who choose to ask CORNERSTONE to **'BIAS'**: During processing, a bias of -35nm will be included in all directions to the layer 404 and the biased area is etched.

Cell Outline – GDS Layer 99

This layer defines the design space boundaries (11.47 x 4.9 mm^2 or 5.5 x 4.9 mm^2).

Labels – GDS Layer 100

This layer defines text labels, which will be merged with Silicon Etch 1 (Grating coupler and Waveguides) by the CORNERSTONE team. **No islands < 20 µm are allowed.** This is because during the HF undercutting process, small features are lifted-off and may redeposit elsewhere on the wafer.

Note: You do not need to add fabrication alignment marks to your design. Layer-to-layer alignment marks will be added by the CORNERSTONE team, placed outside the design area.

4.3 Minimum feature sizes, target critical dimensions and other design rules

- Minimum feature sizes, minimum gaps, and maximum feature widths for each GDS layer are detailed in Table 2.
- The target critical dimension for each GDS layer is listed in Table 2. Note that other feature sizes may have a small dimensional bias.
- **No islands < 20 µm are allowed in GDS layers 404 and 100**. This is because during the HF undercutting process, small features are lifted-off and may redeposit elsewhere on the wafer.
- After HF etch, the expected lateral BOX undercut is 8 µm. Therefore, the maximum width of suspended structures should be 16 µm (see Figure 1).
- Width of the supporting structure/subwavelength structure <6 µm have proven to work (see Figure 1). **If you try more challenging dimensions, do so at your own risk.**
- A minimum spacing between waveguides of at least 75 µm is recommended to avoid suspended waveguides collapsing.
- For gaps in GDS layers 404 and 100 of less than 350 nm, limit the length to a maximum of 20 µm. This is because long, narrow resist features can collapse during resist development.

4.4 Design rules summary

A summary of the design rules and GDS layer numbers described in this section is detailed in Table 2 below.

Table 2 – Design rules summary.

Layer description	Option	GDS no.	Field	Min. feature size	Min. gap	Max. suspended waveguide width	Max. support structure width	Target critical dimension
Silicon Etch 1[¥] (500 nm to BOX layer)	CORNERSTONE NOT to bias	404	Dark	200 nm	250 nm	16 µm[§]	6 µm[α]	230 nm
	CORNERSTONE to bias	404	Dark	270 nm	180 nm	16 µm[§]	6 µm[α]	300 nm
Cell Outline	N/a	99	N/a	N/a	N/a	N/a	N/a	N/a
Labels*[¥]	N/a	100	Dark	250 nm	250 nm	N/a	N/a	N/a

[¥] No islands < 20 µm allowed

[§] After HF etch, the expected lateral BOX undercut is 8 µm. Therefore, the maximum width of suspended structures should be 16 µm (see Figure 1).

[α]Width of the supporting structure/subwavelength structure <6 µm have proven to work (see Figure 1). **If you try more challenging dimensions, do so at your own risk.**

*Features drawn in the Labels layer will be merged into Silicon Etch 1 by the CORNERSTONE team.

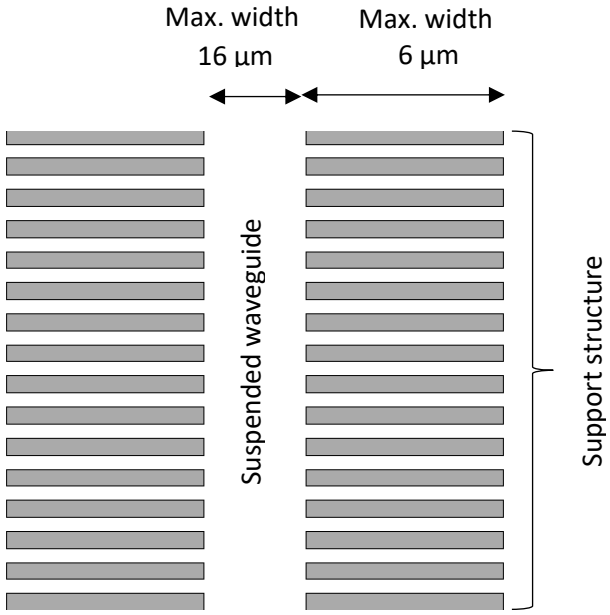


Figure 1: Design rule for suspended and supporting/subwavelength structure maximum width

In order to help you ensure that you comply with the design rules, you can also download a design rule check (DRC) checklist from our website and if you have access to Tanner L-Edit software, a .tdb version of the template containing a DRC file that you can run to automatically find any design rule violations (note that the automatic DRC will not check all of the design rules, so it remains very important to read the design rules in detail).

4.5 File format

Designs must be submitted in a Graphical Database System file format (extension *.gdsII*). Ensure a manufacturing grid size of 1 nm is used.

We recommend dedicated lithography editing software be used in the design of the *.gdsII* file.

4.6 GDSII template file

A *.gdsII* template file has been made available containing the information described in this section. Ensure that all submitted designs fit within the specified area, and that only the designated GDS layer numbers are used.

All components in the *.gdsII* template file are NOT biased. They will be biased by the CORNERSTONE team before fabrication. Therefore, we recommend if you are combining the CORNERSTONE standard components with your own designs that you do not pre-bias your own designs and select the "CORNERSTONE to bias" option when submitting your mask design.

5 Quality assessment

This fabrication run will be qualified by characterising a standard test pattern that is included on the chip (not part of the user cell). The test structures that will be checked after fabrication are reported in Table 3 below, together with the values that are targeted by the CORNERSTONE platform.

Table 3 – Quality assessment parameters.

Test structure	Parameter	Value
Straight single mode suspended waveguide	Propagation loss	< 5 dB/cm for TE mode at λ = 3.8 µm

6 Mask submission procedure

In order to be eligible to submit a design you must first sign-up to this call using the online form found using the link below. This is in order to enable us to prepare the necessary paperwork and plan the fabrication process effectively. The sign-up deadline is found at the top of this document.

www.cornerstone.sotonfab.co.uk/work-with-us/sign-up-form

Under no circumstances will we accept any design submissions for which we have not received a sign-up form.

After completing the sign-up form, when you are ready to submit your mask design on or before the mask submission deadline listed at the top of this document, follow the link below to the CORNERSTONE website mask submission page:

www.cornerstone.sotonfab.co.uk/work-with-us/mask-submission-form

A purchase order (PO) must be uploaded to this form to pay the access fee. Purchase orders will not be accepted via email. If you are from a UK University, then please upload a blank file in place of a PO.

After completion of the mask submission form, within 24 hours you will be emailed a username and password for the online mask uploading module:

https://www.csfm.cornerstone.sotonfab.co.uk/login

Upload your *.gdsII* file to the relevant folder, from where the CORNERSTONE team will be able to access it. Ensure that the top cell in your *.gdsII* file is titled 'Cell0_*[Name of Institution]*'.

Note: Other CORNERSTONE users will not be able to view your uploaded files.

For information about setting up CORNERSTONE as a supplier to your institution, please contact cornerstone@soton.ac.uk.

7 Mask processing performed by CORNERSTONE

Upon receipt of your *.gdsII* file, the CORNERSTONE team will perform the following mask processing steps in order to produce the final mask, based on the descriptions provided in Section 4.2:

Silicon Etch 1 (Waveguide layer) – GDS Layer 404 (Dark field) – etch depth: 500 nm to BOX layer:

1. (**Applicable only for 'BIAS' option**) Shrink Waveguide Etch layer (GDS layer 404) by 35 nm in all directions.
2. Merge the dark field Waveguide Etch layer (GDS layer 404) with Label layer (GDS layer 100).

8 Technical support

If you have any questions relating to the fabrication process or design rules, please contact the CORNERSTONE team (cornerstone@soton.ac.uk).

9 Device delivery

A total of 5 replica cells will be delivered to each user. A tentative delivery date of Friday 29th April 2022 has been set.

10 Feedback

Feedback is essential to the CORNERSTONE team. It is required to ensure a continuous improvement to the quality of our services. It is also evidence on the user satisfaction, and a measure to what extent we were able to meet user requirements. Therefore, we kindly ask our users to provide feedback to us, including device performance data, SEM images, future interests for the CORNERSTONE project etc. A feedback form will be sent to you along with your chips.

Alternatively, email cornerstone@soton.ac.uk with your comments.

11 Publication

Please include CORNERSTONE in the acknowledgments section of any publications that result from the chips you receive from CORNERSTONE.

If you are from a UK University and are receiving your chips free of charge, please also reference the CORNERSTONE 2 funding (EP/T019697/1) in the funding section of your publication.