CORNERSTONE

Quick reference design guidelines for the twelfth fabrication call – February 2019

Sign-up deadline – Friday 15th March 2019

Mask submission deadline – Friday 26th April 2019

File format = *.gdsII*.

Manufacturing grid size = 1 nm.

Design area = **11.47 x 4.9 mm²** or **5.5 x 4.9 mm²**, with 0.5 mm bleed regions on the east and west facets if desired.

Top cell name: 'Cell0_*[Name of Institution]*'.

1. Major changes to design submission process

All design submissions, even those that are supported by EPSRC funding, must agree with the terms and conditions:

www.cornerstone.sotonfab.co.uk/terms-and-conditions

Under no circumstances will we accept designs without agreement with the terms.

Therefore, we strongly recommend that the terms and conditions are pre-authorised by your institution prior to the mask submission date.

Section 7 of the CORNERSTONE 12th Call - Design Rules.pdf document details the design submission process in detail.

2. Design rule changes from previous 340 nm SOI platform call (MPW #7)

The following is a list of design rule changes from the previous 340 nm SOI platform design rules:

1. Minimum feature size for grating coupler layer (GDS layer 6) reduced to 200 nm. Minimum gap set as 250 nm for features up to 20 µm long, and 300 nm for features longer than 20 µm.
2. Minimum feature size for the waveguide layer (GDS layer 3) increased to 350 nm. Minimum gap reduced to 200 nm.
3. New 'labels' layer added as GDS layer 100. This layer will not have any design rule checking (DRC) performed on it and will be merged with Silicon Etch 2 by the CORNERSTONE team.
4. Target critical dimensions for each GDS layer added (Table 1).
5. Step-by-step details of the mask processing steps carried out by the CORNERSTONE team added (Section 8).
6. Standard single mode strip waveguide width for λ = 1.55 µm changed to 450 nm.
7. 1x2 strip MMI for λ = 1.55 µm added.

3. Design rules summary

A summary of the design rules and GDS layer numbers can be found in Table 1 below.

Table 1 – Design rules summary.

Layer description	GDS number	Field	Min. feature size	Min. gap	Max. feature width	Target critical dimension
Silicon Etch 1 (140 nm ± 10 nm)	6	Dark	200 nm	250 nm	20 µm	265 nm
			200 nm	300 nm	N/a	
Silicon Etch 2 (340 nm to BOX)	3	Light	350 nm	200 nm	N/a	450 nm
	4	Dark	200 nm	350 nm		
Heater Filaments	39	Light	900 nm	10 µm	N/a	900 nm
Heater Contact Pads	41	Light	2 µm	10 µm	N/a	2 µm
Bleed Area	98	N/a	N/a	N/a	N/a	N/a
Cell Outline	99	N/a	N/a	N/a	N/a	N/a
Labels*	100	Dark	250 nm	250 nm	N/a	N/a

*Features drawn in the Labels layer will be merged into Silicon Etch 2 by the CORNERSTONE team.

4. Minimum feature sizes, tolerances and other design rules

- Minimum feature sizes, minimum gaps, and maximum feature widths for each GDS layer are detailed in Table 1.
- The target critical dimension for each GDS layer is listed in Table 1. Note that other feature sizes may have a small dimension bias.
- A minimum spacing between waveguides of at least 5 µm is recommended to avoid power coupling.
- An overlap of at least 200 nm between GDS layers is essential to account for the alignment tolerance between layers.
- All structures drawn in GDS layer 6 (Grating couplers) must overlap by at least 200 nm with GDS layer 3 (Waveguides).
- An overlap of at least 10 µm between GDS layer 39 (Heater Filaments) and GDS layer 41 (Heater Contact Pads) is recommended for optimal heater performance.
- Ensure all structures drawn in GDS layer 6 (Grating couplers) do not overlap with either GDS layer 39 (Heater Filaments) or GDS 41 (Heater Contact Pads).

5. Technical support

For all queries, email cornerstone@soton.ac.uk.