Cornerstone

Design guidelines for the first fabrication call – December 2016

1. File format

Designs must be submitted in a Graphical Database System file format (extension .gdsII).

2. Design rules

It is important that designs conform to the following design rules to ensure clarity and correct processing. For this first call, we will process chips with a 220 nm-thick silicon core on a 3 µm -thick BOX (Buried OXide) layer. We will offer two etch processes: 1) a shallow silicon etching of 70 nm, and 2) a deep silicon etching of 220 nm to the BOX layer.

2.1. GDS Layers

Each lithographic step in the fabrication process flow is identified by a specific GDS layer. These are as follows:

GDS layer 6 – Silicon Etch 1 (Grating couplers)

This layer is used to define grating couplers, which are fabricated with the 70 nm shallow silicon etching. Positive tone e-beam resist is used, therefore the drawn area is etched.

GDS layer 3 – Silicon Etch 2 (Waveguiding layer)

This layer defines the waveguiding layer. Drawn objects on this layer will be protected from the silicon etch. User should draw the waveguides and any other features to remain following etching to the bulk SiO_2. During fracturing processing for the e-beam, this will be translated into a pattern which defines 5 µm-wide trenches on either side of the waveguide which will eventually be etched.

Note: You do not need to add fabrication alignment markers to your design

2.2 Minimum feature sizes and tolerances

Patterns should have a minimum feature size of no less than 150 nm. If required, smaller features, down to 100 nm, can be patterned but the etching depth within sub-150 nm gaps cannot be accurately controlled.

A minimum spacing between waveguides of at least 5 µm is recommended to avoid power coupling.

2.3 Design area

The standard user cell has a dimension of **7 x 7 mm²**. If cleaved facets are required for edge coupling the total writing area is reduced to 7 x 6 mm² as an overlay (or bleed) of 500 µm should be included as shown in Fig.1. Please note that the input/output waveguides should extend into the bleed area.

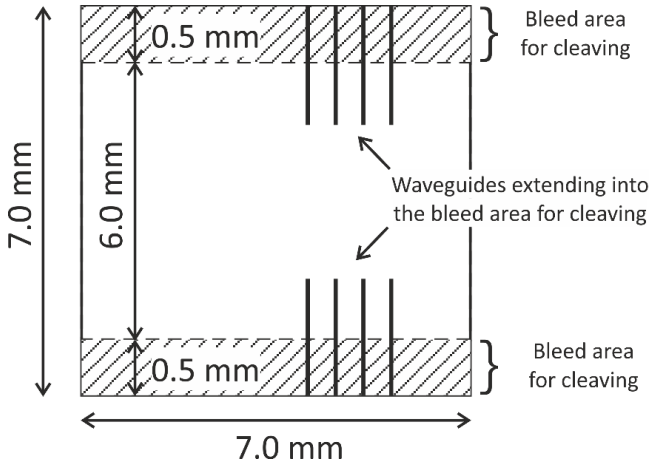


Figure 1. User cell design area layout

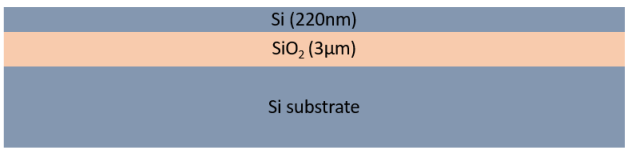
3. Process flow

The patterns will be processed by e-beam lithography on a single-side polished Silicon-on-Insulator (SOI) wafer, with the following nominal parameters:

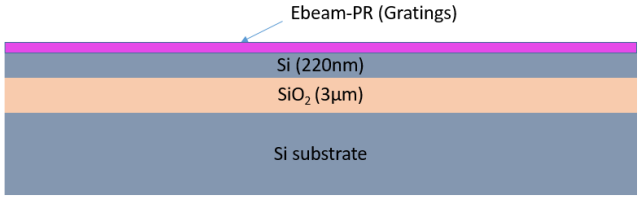
- Crystalline silicon (Si) substrate with a thickness h_{sub} = 675 ± 15 µm
- Thermal silica (SiO_2) BOX layer with a thickness h_{box} = 3 µm;
- Crystalline silicon (Si) core layer with a thickness h_{wg} = 220 nm.

The schematic description of the process flow is given below:

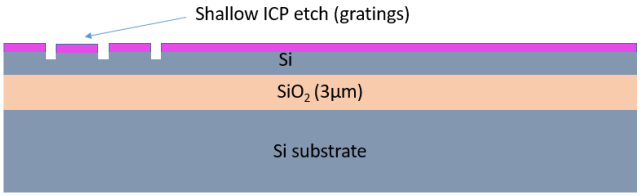
1) Starting with a bare SOI wafer



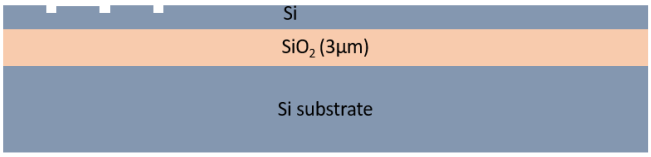
2) E-beam patterning for Silicon Etch 1 (GDS layer 6) – shallow etch



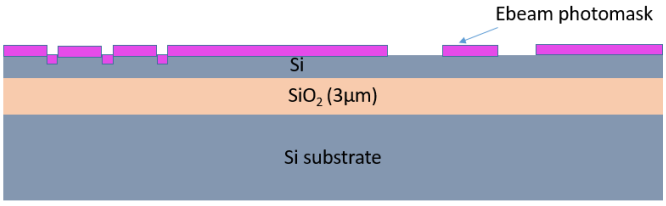
3) Shallow ICP Silicon etch (70 nm etch depth)



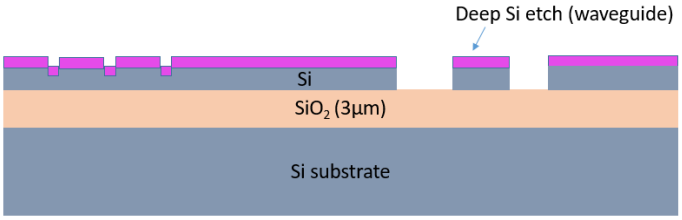
4) E-beam resist strip



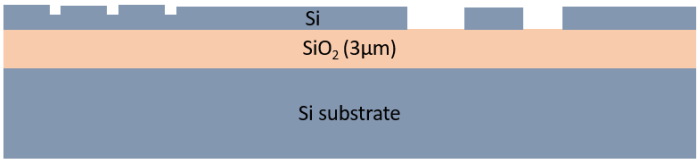
5) E-beam patterning for Silicon Etch 2 (GDS layer 3) – deep etch



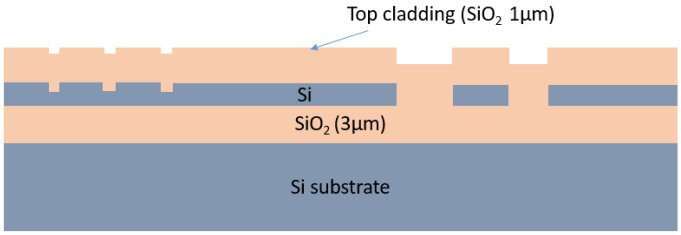
6) Deep ICP Silicon etch (220 nm) – all the way to BOX layer



7) E-beam resist strip



8) Deposition of a 1 µm-thick silicon dioxide top cladding



Please note that the deposition of the silicon dioxide top cladding is optional.

4. Quality Assessment

Each fabrication run will be qualified by characterising a number of test patterns that are included on the chip (these are not part of the user cell). The list of the optical parameters that will be checked after each run is reported in the table below, together with the optical values that are guaranteed by the Cornerstone platform.

Test structure	**Parameter**	**Value (Max)**
Straight waveguides	Propagation loss	<4 dB/cm for TE mode
APF ring resonators	Group effective index	< 5e-3 over 1 x1 mm^2

5. Technical support

If you have any questions relating to the fabrication process or design rules please contact the Cornerstone coordinator Stevan Stanković (S.Stankovic@soton.ac.uk) or Graham Sharp (Graham.Sharp@glasgow.ac.uk).

Several standard components such as single mode waveguides, surface gratings, ring resonators, waveguide couplers, Mach-Zehnder interferometers have already been designed and assessed by the Cornerstone consortium. Please contact the consortium coordinator should you require the *.gdsII* cells or more information on specific component performance.