CORNERSTONE MPW DESIGN RULES:
340 nm SOI MPW #40 September 2024

SIGN-UP DEADLINE: 27/09/2024 **MASK SUBMISSION DEADLINE:** 23/10/2024

1 TERMS & CONDITIONS AND COST

All design submissions must agree with the terms and conditions:

www.cornerstone.sotonfab.co.uk/terms-and-conditions

Under no circumstances will we accept designs without agreement with the terms.

Therefore, we strongly recommend that the terms and conditions are pre-authorised by your institution prior to the mask submission date.

A purchase order (PO) must be uploaded at the same time as submitting your mask design in order pay the access fee, detailed in *Table 1* below. Purchase orders will not be accepted via email.

Table 1 – Access cost and delivery time.

Design Area [mm²]	11.47 x 4.9	5.5 x 4.9	Delivery Time
Access Cost with Heaters (Priority)*	£17,900	£13,200	7 weeks
Access Cost without Heaters (Priority)*	£11,300	£ 7,900	5 weeks
Access Cost with Heaters (Standard)*	£14,250	£10,500	14 weeks
Access Cost without Heaters (Standard)*	£ 9,000	£ 6,250	14 weeks
Access cost for staff and students employed at UK Universities (Standard)**	£0	£0	14 weeks
Access cost for enterprises based in UK†	50% off	50% off	As above

*Quoted prices are exclusive of VAT, import duties/customs fees, withholding taxes etc.

** Access costs for staff and students employed at UK Universities is funded under the Engineering and Physical Sciences Research Council (EPSRC) CORNERSTONE 2.5 project (EP/W035995/1). Free-of-charge access is limited to 1 design area per research group.

†Are you a UK company?

UK companies may be eligible for a 50% discount on the cost of this MPW run with support from the CORNERSTONE Photonics Innovation Centre (C-PIC) (EP/Z531066/1), funded by UK Research and Innovation. Support will be provided under the Subsidy Control Act (2022) via Minimal Financial Assistance. To be eligible you will need to demonstrate the potential impact of receiving assistance against one or more of the following categories: impact on jobs and skills, access to new technology, accelerating product development. Following submission of your sign-up form, you will receive correspondence with more details of how this support will be provided. The support is only available to UK companies using CORNERSTONE for prototyping and product development.

Priority batches are designed to accelerate delivery times by utilizing expedited services for obtaining reticles, prioritizing access to cleanroom tools, working out-of-hours, and simplifying intermittent quality checks during the fabrication process, instead relying on the inherent repeatability of the lithography and etching processes. Additionally, the submitted layouts will not undergo further inspection against design rules after the submission deadline. Consequently, users opting for the priority option are required to submit designs that pass the Design Rule Check (DRC) on or before the submission deadline. The CORNERSTONE team would be grateful for the opportunity to work with you prior to the submission deadline to ensure your designs pass DRC. For more information, please visit our website: www.cornerstone.sotonfab.co.uk/design-rules

For information about setting up CORNERSTONE as a supplier to your institution, please contact cornerstone@soton.ac.uk.

2. DESIGN RULE CHANGES FROM PREVIOUS CALL (SOI 340nm MPW #36)

- Shallow etched rib waveguide added.
- Rib-to-strip transition design added to component library.
- Thermal isolation trench for heaters introduced.
- Heater with thermal isolation trench design added to component library.

3. IPKISS PROCESS DESIGN KIT

For the greatest functionality, we recommend that you use Luceda's IPKISS software to access the process design kit (PDK), after purchasing the required license. The IPKISS platform enables the automation and integration of all aspects of your photonic design flow in one tool, using one standard language. The PDK can be used in either IPKISS' Python coding environment or in the GUI of Siemens EDA L-Edit by using the IPKISS Link for Siemens EDA.

To obtain a copy of the software and a license key, please contact Luceda by sending an email to info@lucedaphotonics.com, specifying that you require a license for CORNERSTONE PDK usage. Luceda will contact you within 1-2 working days following the receipt of your request to provide a quote for the license. Of course, if you already have a valid license, the PDK can be accessed free of charge.

For more information, please visit www.lucedaphotonics.com.

Once you have access to the Luceda software, in order to obtain a copy of the CORNERSTONE PDK, please contact Luceda support at info@lucedaphotonics.com. An account will be created for you at support.lucedaphotonics.com for any technical support on Luceda's IPKISS software or the CORNERSTONE PDK implementation.

We also have a PDK available for download in .gdsII format.

4. PROCESS FLOW

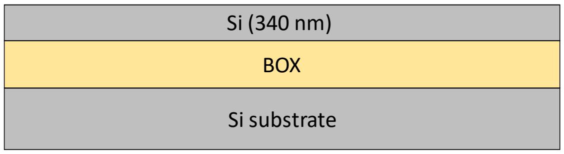
For this call, the patterns will be processed on a single-side polished Silicon-on-Insulator (SOI) wafer, with the following nominal parameters:

- Crystalline silicon (Si) substrate with the resistivity of 750 Ω.cm
- Thermal silica (SiO_2) Buried OXide (BOX) layer with a thickness h_{box} = 2 µm
- Crystalline silicon (Si) core layer (100)-oriented with a thickness h_{wg} =340 nm ±20 nm

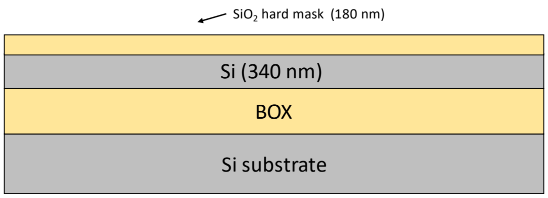
We will offer two silicon etch processes: 1) a shallow silicon etch of 140 nm ± 10 nm, and 2) a full silicon etch to the BOX layer. We will offer a 1 µm ± 100 nm thick silicon dioxide top cladding layer with two metal layers for heaters: 1) heater filaments, and 2) heater contact pads. Finally, we will offer etched trenches to the silicon substrate for thermal isolation.

The schematic description of the process flow is given below:

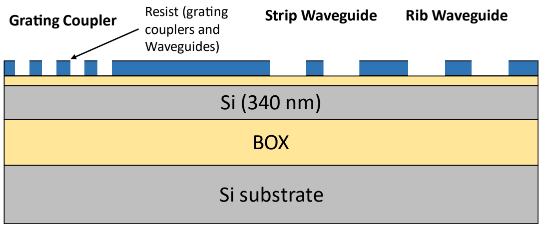
1. Starting SOI substrate



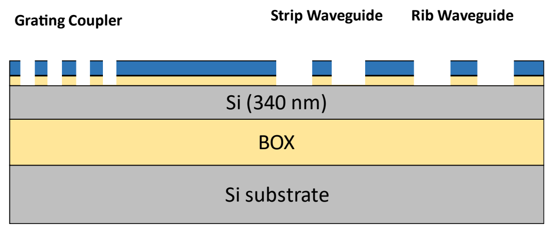
2. Silicon dioxide hard mask deposition – 180 nm



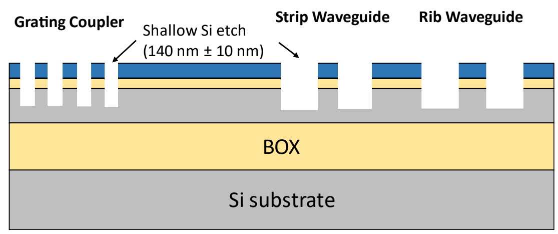
3. Resist patterning for Silicon Etch 1 (GDS layer 3, 4 & 6) – 140 nm ± 10 nm etch



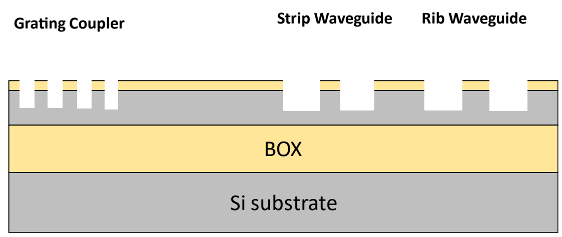
4. Hard mask etch



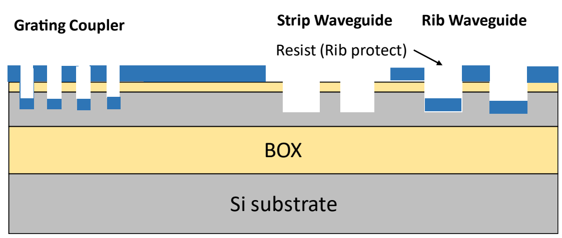
5. Shallow Si etch (140 nm ± 10 nm etch depth)



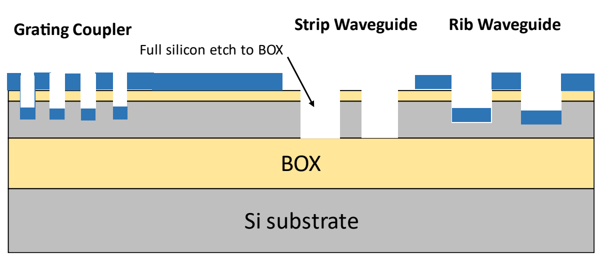
6. Resist strip



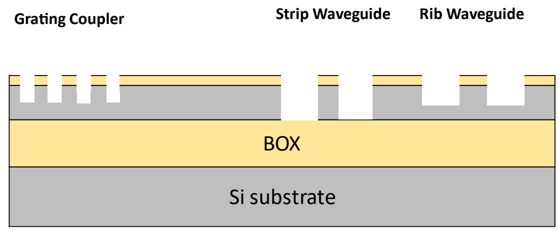
7. Resist patterning for Silicon Etch 2 (GDS layer 5) – 200 nm etch to BOX



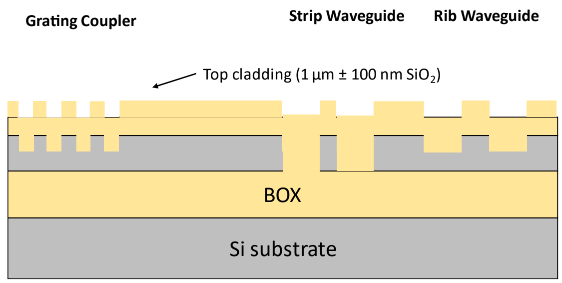
8. Rib-to-strip Si etch (200 nm to BOX)



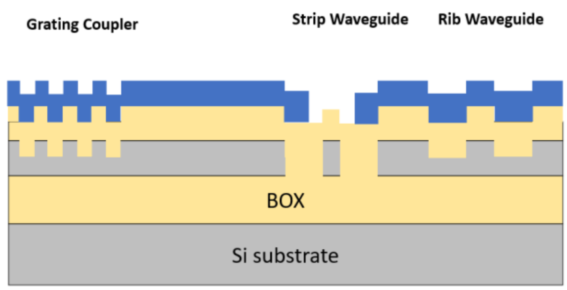
9. Resist strip



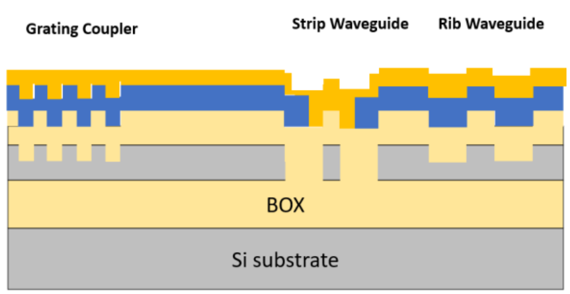
10. Deposition of 1 µm ± 100 nm thick SiO_2 top cladding



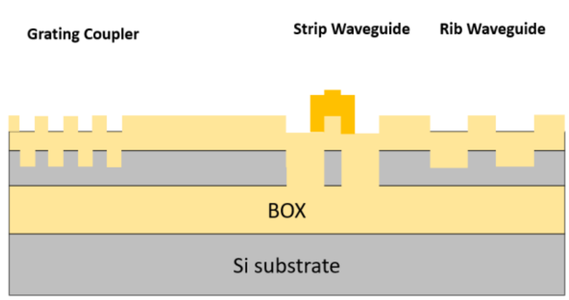
11. Resist patterning for Heater Filaments (GDS layer 39)



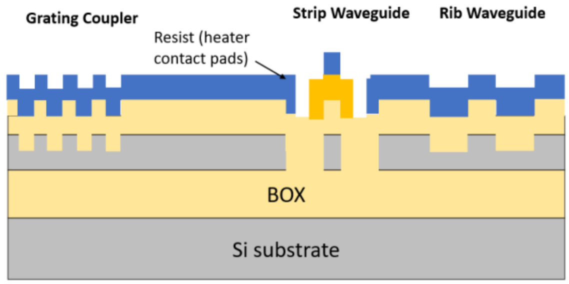
12. Heater filament deposition



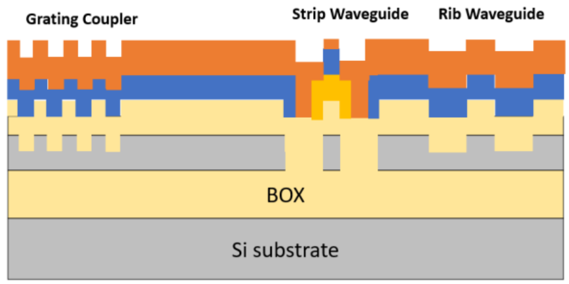
13. Metal lift-off



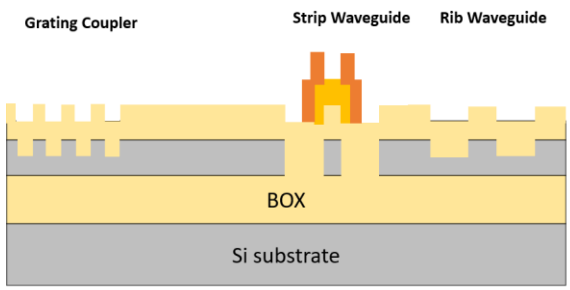
14. Resist patterning for Heater Contact Pads (GDS layer 41)



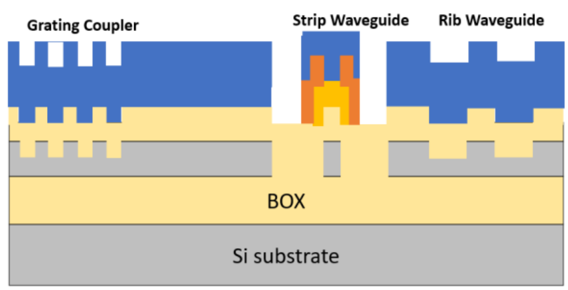
15. Heater contact pads deposition



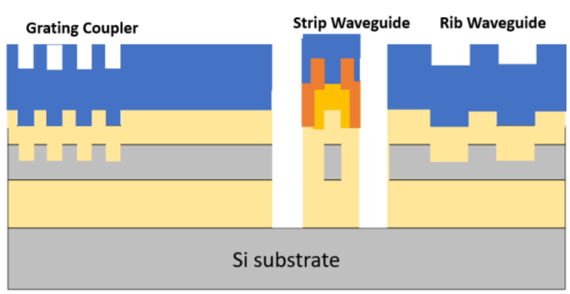
16. Metal lift-off



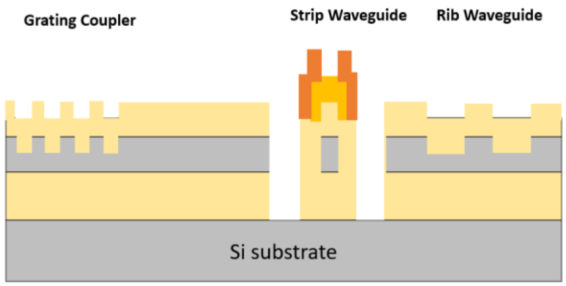
17. Resist patterning for heater isolation trench (GDS layer 46)



18. Silicon dioxide etching to the silicon substrate



19. Resist strip



If you require any alternative processing steps (e.g. custom etch depths), we may be able to perform them for a suitable charge. Email cornerstone@soton.ac.uk with your request.

5. DESIGN RULES

It is important that designs conform to the following design rules to ensure clarity and correct processing.

5.1 DESIGN AREA

The standard user cell has dimensions of **11.47 x 4.9 mm²** or **5.5 x 4.9 mm²**.

5.1.1 PHYSICAL DIE SIZE

The physical size of the dies you will receive is approximately 5.3-5.6 x 12.5 mm^2. This area includes a border the CORNERSTONE team will add that contains alignment marks, metrology boxes etc. which surround 3x design areas from various CORNERSTONE users, as shown in Figure 1. If you require specific physical die dimensions (5.3 x 12.5 mm^2 or 5.6 x 12.5 mm^2), for example if integration to a PCB is required, please specify the physical die dimensions you require in the online mask submission form you are required to complete as part of the submission process (see Section 8).

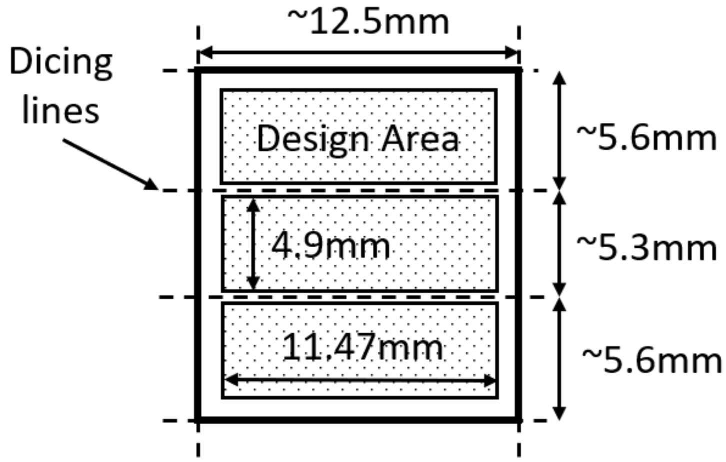


Figure 1– Physical die dimensions.

5.2 GDS LAYERS

Each lithographic step in the fabrication process flow is identified by a specific GDS layer/s. These are as follows:

Silicon Etch 1 (Grating & Waveguide layer) – GDS Layer 3 (Waveguide Light field), GDS Layer 4 (Waveguide Dark field) & GDS Layer 6 (Gratings Dark field)- etch depth: 140 nm ± 10 nm

This layer is used to define grating couplers as well as both strip and rib waveguides (to form a rib waveguide, the slab region is protected during Silicon Etch 2, defined by GDS layer 5 – see below), and is split into three separate GDS layer numbers, patterned into the same resist and etched together:

GDS Layer 3: Drawn objects on this layer will be protected from the silicon etch. Users should draw the waveguides and any other features to remain following silicon etching. During fracturing processing, this will be translated into a pattern that defines 5 µm wide trenches on either side of the waveguides drawn in GDS layer 3 (see Figure 2).

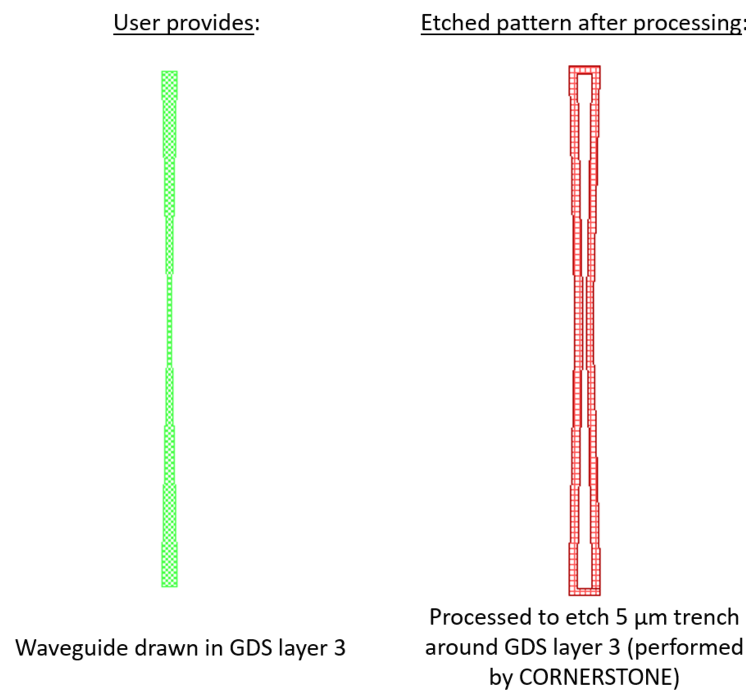


Figure 2 – Description of GDS Layer 3 processing.

If you require waveguide trenches that are a different width, refer to the guidelines for generating the trenches in Section 9. You can complete these steps yourself and modify the growth function dimension in step 1.

GDS Layer 4: Drawn objects on this layer will be exposed to silicon etching. An example photonic crystal structure is shown in Figure 3. The important thing to note here is that the waveguide layer drawn in GDS layer 3 should overlap the structures drawn in GDS layer 4, so that when the 5 µm trenches are generated by CORNERSTONE, a continuous waveguide remains.

GDS Layer 6: Drawn objects on this layer will be exposed to silicon etch to define grating couplers, which are fabricated with 140 nm shallow silicon etching. The drawn area is etched.

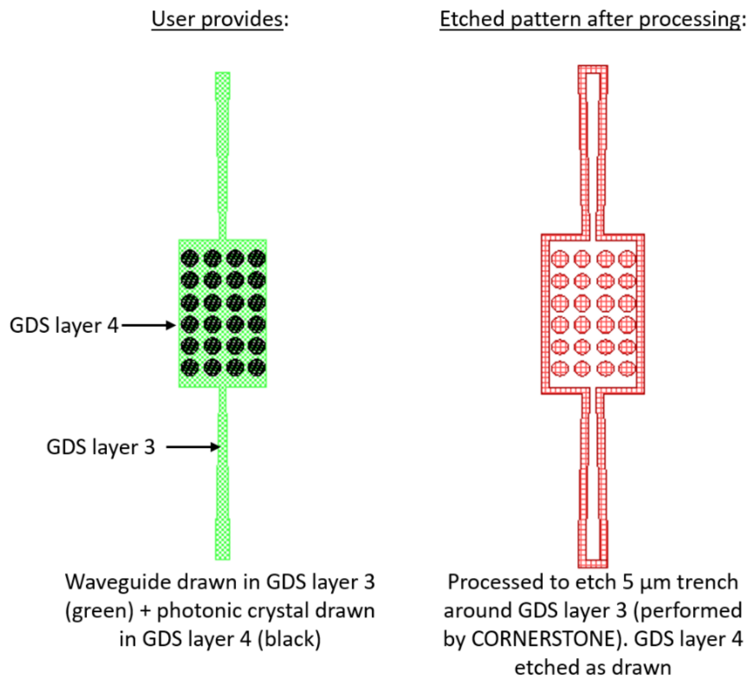


Figure 3 – Example photonic crystal structure using GDS Layers 3 & 4.

Silicon Etch 2 (Rib protect layer) – GDS Layer 5 (Light field) – etch depth: 200 nm to BOX

This layer defines the protective layer for rib waveguides. Drawn objects in this layer will be protected from etching whilst the strip waveguides are etched to the BOX (all areas not previously defined in the Silicon Etch 1 layer will be protected from etching by a hard mask). We recommend that this layer should extend more than or equal to 5 µm from the edge of features drawn in GDS layer 3 so that the 5 µm wide trenches etched in the previous partial silicon etching step are fully protected by GDS layer 5, with the exception of any rib-to-strip transitions. An overview of how to draw both strip and rib waveguides is shown in Figure 4.

All grating couplers (GDS layer 6) should also be protected with GDS layer 5.

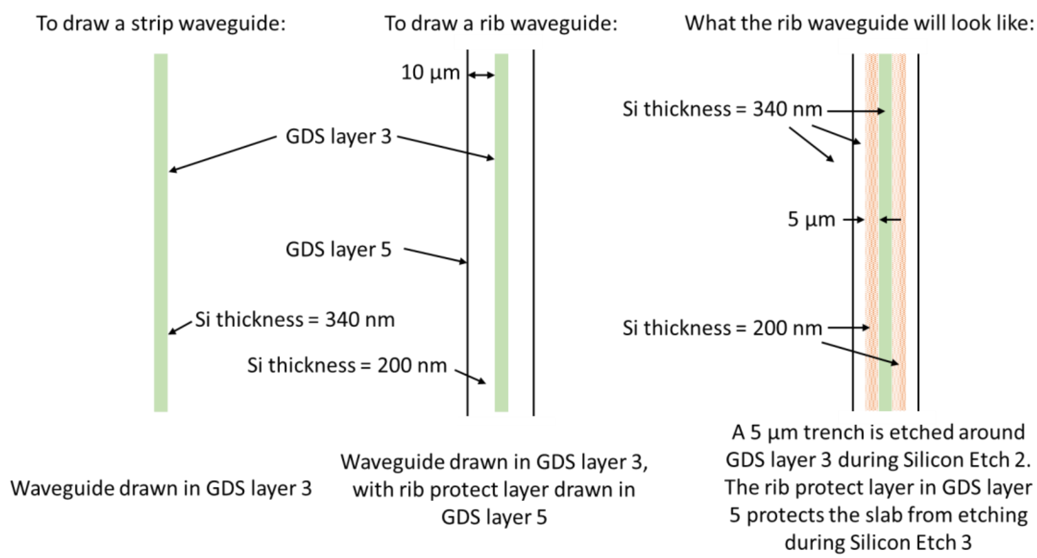


Figure 4 – Drawing strip and rib waveguides.

Heater Filaments – GDS Layer 39 (Light field)

This layer defines the heater filaments. Drawn objects on this layer will remain after metal lift-off. It is recommended to use a filament width of 900 nm for the best compromise between heater power efficiency and phase tunability.

Heater Contact Pads – GDS Layer 41 (Light field)

This layer defines the heater contact pads. Drawn objects on this layer will remain after metal lift-off.

An example heater layout for a straight waveguide is included in the *.gdsII* template file. The contact pads can be modified according to your probe design.

Isolation Trenches – GDS Layer 46 (Dark field)

This layer defines deep etched isolation trenches around the heater filaments (GDS layer 39). Drawn objects in this layer will be exposed to silicon dioxide etching to the Si substrate.

Cell Outline – GDS Layer 99

This layer defines the design space boundaries (11.47 x 4.9 mm^2 or 5.5 x 4.9 mm^2).

Labels – GDS Layer 100

This layer defines text labels, which will be merged with Silicon Etch 1 (Waveguides) by the CORNERSTONE team. This layer will not have any design rule checking (DRC) performed.

Note: You do not need to add fabrication alignment marks to your design. Layer-to-layer alignment marks will be added by the CORNERSTONE team, placed outside the design area.

5.3 MINIMUM FEATURE SIZES, TARGET CRITICAL DIMENSIONS AND OTHER DESIGN RULES

- Minimum feature sizes, minimum gaps, and maximum feature widths for each GDS layer are detailed in *Table 2*.
- The target critical dimension for each GDS layer is listed in *Table 2*. Note that other feature sizes may have a small dimensional bias.
- A minimum spacing between waveguides of at least 5 µm is recommended to avoid power coupling.
- An overlap of at least 200 nm between GDS layers is essential to account for the alignment tolerance between layers.
- All structures drawn in GDS layer 6 (if they are grating couplers) must overlap by at least 200 nm with GDS layer 3 (Waveguides) to account for alignment errors, and with GDS layer 5 (rib protect layer) to prevent the grating couplers becoming fully etched during Silicon Etch 2.
- An overlap of at least 10 µm between GDS layer 39 (Heater Filaments) and GDS layer 41 (Heater Contact Pads) is recommended for optimal heater performance.
- Ensure all structures drawn in GDS layer 6 (if they are grating couplers) do not overlap with either GDS layer 39 (Heater Filaments) or GDS 41 (Heater Contact Pads).

- GDS layer 46 should not overlap with Waveguides (GDS layer 3) & there should be a minimum distance between GDS layer 46 and GDS layer 3 of 200 nm.
- GDS layer 46 should not overlap with Heater Filaments (GDS layer 39) & there should be a minimum distance between GDS layer 46 and GDS layer 39 of 200 nm.
- GDS layer 46 should not overlap with Heater Contact Pads (GDS layer 41) & there should be a minimum distance between GDS layer 46 and GDS layer 41 of 200 nm.

5.4 DESIGN RULES SUMMARY

A summary of the design rules and GDS layer numbers described in this section is detailed in *Table 2* below.

Table 2 – Design rules summary

Layer description	GDS number	Field	Min. feature size	Min. gap	Max. feature width	Target critical dimension
Silicon Etch 1 (140 nm ± 10 nm)	3	Light	350 nm	200 nm	N/a	265 nm
	4	Dark	200 nm	350 nm	N/a	
	6	Dark	200 nm	250 nm	20 µm	
			200 nm	350 nm	N/a	
Silicon Etch 2 (200 nm to BOX)	5	Light	350 nm	200 nm	N/a	450 nm
Heater Filaments	39	Light	600 nm	10 µm	N/a	900 nm
Heater Contact Pads	41	Light	2 µm	10 µm	N/a	2 µm
Isolation trench	46	Dark	5 µm	2 µm	N/a	5 µm
Cell Outline	99	N/a	N/a	N/a	N/a	N/a
Labels*	100	Dark	250 nm	250 nm	N/a	N/a

*Features drawn in the Labels layer will be merged into Silicon Etch 1 by the CORNERSTONE team.

In order to help you ensure that you comply with the design rules, you can download and execute the KLayout pre-DRC script provided by CORNERSTONE on our website www.cornerstone.sotonfab.co.uk/design-rules (note that the automatic DRC will not check all of the design rules, so it remains very important to read the design rules in detail).

For users choosing the priority option, it is essential to provide DRC-free mask layouts on or before the submission deadline. Therefore, users planning to initiate a priority batch should run the L-edit DRC file and confirm that the submitted design is free of design rule issues before the submission deadline. The CORNERSTONE team will not undertake post-submission DRC for priority access users to shorten the delivery timeline.

MPW users will have an opportunity to attend 1-to-1 Drop-in Sessions to pre-review mask layouts before the submission deadline, using this link to book a 20-min session.

5.5 FILE FORMAT

Designs must be submitted in a Graphical Database System file (extension *.gdsII*) or Open Artwork System Interchange Standard (extension *.oas*) format. Ensure a manufacturing grid size of 1 nm is used, as per the CORNERSTONE GDSII Template file.

We recommend dedicated lithography editing software be used in the design of the *.gdsII* or *.oas* file.

5.6 GDSII TEMPLATE FILE

A *.gdsII* template file has been made available on our website containing the information described in this section. Ensure that all submitted designs fit within the specified area, and that only the designated GDS layer numbers are used.

6 MATERIAL PROPERTIES

The measured refractive indices of the Silicon and SiO_2 layers are shown in Figure 4 below. This data is also available in tabular format on our website.

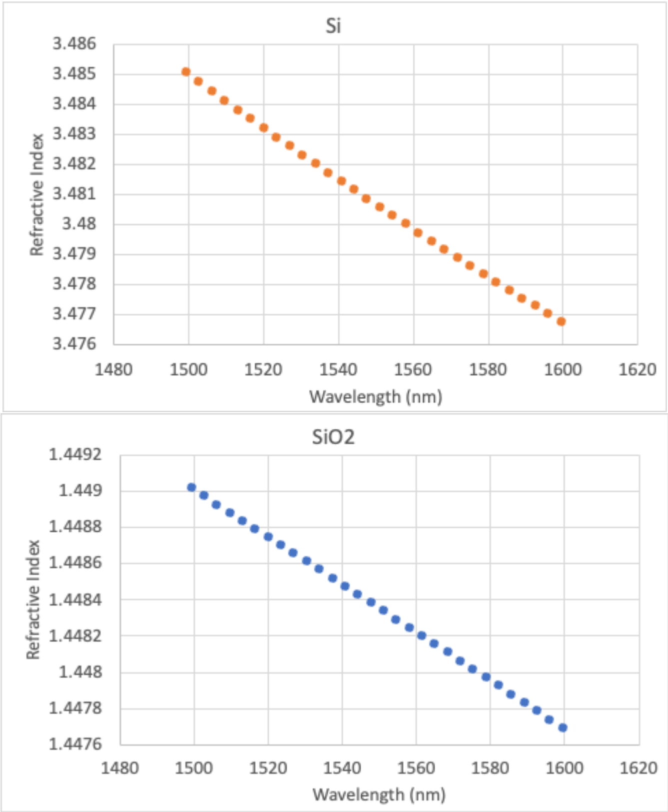


Figure 4 – Refractive indices of Silicon(upper) and SiO_2 (bottom).

7 QUALITY ASSESSMENT

This fabrication run will be qualified by characterising a standard test pattern that is included on the chip (not part of the user cell). The test structures that will be checked after fabrication are reported in Table 3 below, together with the values that are targeted by the CORNERSTONE platform.

Table 3 – Quality assessment parameters.

Test structure	Parameter	Value
Straight single mode strip waveguide	Propagation loss	< 5 dB/cm for TE mode
Straight single mode rib waveguide	Propagation loss	< 1.5 dB/cm for TE mode
MZI integrated with the PDK heater	Phase shift efficiency	< 30 mW/π
MZI integrated with the PDK heater with isolation trench	Phase shift efficiency	< 15 mW/π

8 MASK SUBMISSION PROCEDURE

In order to be eligible to submit a design you must first sign-up to this call using the online form found using the link below. This is in order to enable us to prepare the necessary paperwork and plan the fabrication process effectively. The sign-up deadline is found at the top of this document.

www.cornerstone.sotonfab.co.uk/mpw-sign-up-form

Under no circumstances will we accept any design submissions for which we have not received a sign-up form.

After completing the sign-up form, when you are ready to submit your mask design on or before the mask submission deadline listed at the top of this document, follow the link below to the CORNERSTONE website mask submission page:

www.cornerstone.sotonfab.co.uk/gds-file-upload

A purchase order (PO) must be uploaded to this form to pay the access fee. Purchase orders will not be accepted via email. If you are accessing this call free of charge, benefitting from the CORNERSTONE 2.5 funding, simply upload a blank file.

You must also upload your design file to the submission form. Ensure that the top cell in your design file is titled 'Cell0_*[Name of Institution]*'.

For information about setting up CORNERSTONE as a supplier to your institution, or if you encounter any problems with the online forms, please contact cornerstone@soton.ac.uk.

9 MASK PROCESSING PERFORMED BY CORNERSTONE

Upon receipt of your *.gdsII* file, the CORNERSTONE team will perform the following mask processing steps in order to produce the final mask, based on the descriptions provided in Section 5.2:

Silicon Etch 1 (Grating & Waveguide layer) – GDS Layer 3 (Light field), GDS Layer 4 (Dark field), GDS Layer 6 (Dark field) & GDS Layer 100 (Dark field) – etch depth: 140 nm ± 10 nm:

1. Grow Waveguide layer (GDS layer 3) by 5 µm in all directions.
2. Subtract the Waveguide layer (GDS layer 3) from the output of (1) to produce the etch trenches around the drawn waveguides.

3. Merge the output of (2) with the dark field Waveguide Etch layer (GDS layer 4), Grating Etch layer (GDS layer 6), Heater Isolation Trench layer (GDS layer 46) and the Labels layer (GDS layer 100).

Silicon Etch 2 (Rib protect layer) – GDS Layer 5 (Light field) – etch depth: 200 nm to BOX:

1. Temporarily, grow the Grating Coupler layer (GDS layer 6) by 200 nm in all directions.
2. Copy the output from (1) into the Rib Protect layer (GDS layer 5).
3. Subtract the output of (2) from the Cell Outline (GDS layer 99) to convert to a dark field mask.
4. Subtract the heater isolation trenches (GDS layer 46) from the output of (3).

10. TECHNICAL SUPPORT

If you have any questions relating to the fabrication process or design rules, please contact the CORNERSTONE team (cornerstone@soton.ac.uk).

11. CHIP DELIVERY

A total of 10 replica cells will be delivered to each user. The delivery time schedule can be found in Table 1.

12. FEEDBACK

Feedback is essential to the CORNERSTONE team. It is required to ensure a continuous improvement to the quality of our services. It is also evidence on the user satisfaction, and a measure to what extent we were able to meet user requirements. Therefore, we kindly ask our users to provide feedback to us, including device performance data, SEM images, future interests for the CORNERSTONE project etc. A feedback form will be sent to you along with your chips.

Alternatively, email cornerstone@soton.ac.uk with your comments.

13. PUBLICATIONS

If you are benefitting from free-of-charge access via the CORNERSTONE 2.5 funding, please include the following statement in the "Funding" section of any publications:

"The chip fabrication for this research was funded by the Engineering and Physical Sciences Research Council (EPSRC) CORNERSTONE 2.5 (EP/W035995/1) project."

If you are benefitting from subsidised access via the C-PIC funding, please include the following statement in the "Funding" section of any publications:

"The chip fabrication for this research was funded by the Engineering and Physical Sciences Research Council (EPSRC) C-PIC (EP/Z531066/1) project."

This is important to us to be able to demonstrate impact from the funding.

If you are a paying user, we kindly ask that you include CORNERSTONE in the "Acknowledgments" section of any publications that result from the chips you receive from CORNERSTONE.