CORNERSTONE MPW DESIGN RULES:
Suspended-Si MPW #6 September 2024

SIGN-UP DEADLINE: 04/10/2024 **MASK SUBMISSION DEADLINE:** 30/10/2024

1 TERMS & CONDITIONS AND COST

All design submissions must agree with the terms and conditions:

www.cornerstone.sotonfab.co.uk/terms-and-conditions

Under no circumstances will we accept designs without agreement with the terms.

Therefore, we strongly recommend that the terms and conditions are pre-authorised by your institution prior to the mask submission date.

A purchase order (PO) must be uploaded at the same time as submitting your mask design in order pay the access fee, detailed in *Table 1* below. Purchase orders will not be accepted via email.

Table 1 – Access cost and delivery time.

Design Area [mm²]	11.47 x 4.9	5.5 x 4.9	Delivery Time
Access Cost (Priority)*	£13,750	£9,700	5 weeks
Access Cost (Standard)*	£11,000	£7,750	10 weeks
Access cost for staff and students employed at UK Universities**	£0	£0	10 weeks
Access cost for enterprises based in UK†	50% off	50% off	As above

*Quoted prices are exclusive of VAT, import duties/customs fees, withholding taxes etc.

** Access costs for staff and students employed at UK Universities is funded under the Engineering and Physical Sciences Research Council (EPSRC) CORNERSTONE 2.5 project (EP/W035995/1). Free-of-charge access is limited to 1 design area per research group.

†**Are you a UK company?**

UK companies may be eligible for a 50% discount on the cost of this MPW run with support from the CORNERSTONE Photonics Innovation Centre (C-PIC) (EP/Z531066/1), funded by

UK Research and Innovation. Support will be provided under the Subsidy Control Act (2022) via Minimal Financial Assistance. To be eligible you will need to demonstrate the potential impact of receiving assistance against one or more of the following categories: impact on jobs and skills, access to new technology, accelerating product development. Following submission of your sign-up form, you will receive correspondence with more details of how this support will be provided. The support is only available to UK companies using CORNERSTONE for prototyping and product development.

Priority batches are designed to accelerate delivery times by utilizing expedited services for obtaining reticles, prioritizing access to cleanroom tools, working out-of-hours, and simplifying intermittent quality checks during the fabrication process, instead relying on the inherent repeatability of the lithography and etching processes. Additionally, the submitted layouts will not undergo further inspection against design rules after the submission deadline. Consequently, users opting for the priority option are required to submit designs that pass the Design Rule Check (DRC) on or before the submission deadline. The CORNERSTONE team would be grateful for the opportunity to work with you prior to the submission deadline to ensure your designs pass DRC. For more information, please visit our website: www.cornerstone.sotonfab.co.uk/design-rules

For information about setting up CORNERSTONE as a supplier to your institution, please contact cornerstone@soton.ac.uk.

2. DESIGN RULE CHANGES FROM PREVIOUS CALL (MPW #5)

- Partial Si etch process added.
- Rib waveguides added to GDS template.

3. IPKISS PROCESS DESIGN KIT

For the greatest functionality, we recommend that you use Luceda's IPKISS software to access the process design kit (PDK), after purchasing the required license. The IPKISS platform enables the automation and integration of all aspects of your photonic design flow in one tool, using one standard language. The PDK can be used in either IPKISS' Python coding environment or in the GUI of Siemens EDA L-Edit by using the IPKISS Link for Siemens EDA.

To obtain a copy of the software and a license key, please contact Luceda by sending an email to info@lucedaphotonics.com, specifying that you require a license for CORNERSTONE PDK usage. Luceda will contact you within 1-2 working days following the receipt of your request to provide a quote for the license. Of course, if you already have a valid license, the PDK can be accessed free of charge.

For more information, please visit www.lucedaphotonics.com.

Once you have access to the Luceda software, in order to obtain a copy of the CORNERSTONE PDK, please contact Luceda support at info@lucedaphotonics.com. An account will be created for you at support.lucedaphotonics.com for any technical support on Luceda's IPKISS software or the CORNERSTONE PDK implementation.

We also have a PDK available for download in .gdsII format.

4. PROCESS FLOW

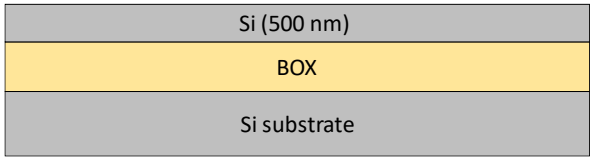
For this call, the patterns will be processed on a single-side polished Silicon-on-Insulator (SOI) wafer, with the following nominal parameters:

- Crystalline silicon (Si) substrate with the resistivity of 750 Ω.cm
- Thermal silica (SiO_2) Buried OXide (BOX) layer with a thickness h_{box} = 3 µm
- Crystalline silicon (Si) core layer (100)-oriented with a thickness h_{wg} = 500 nm ± 15 nm

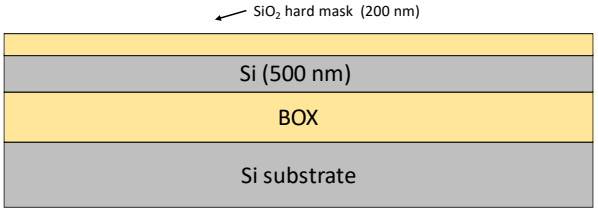
We will offer two silicon etch processes: 1) a partial silicon etch of 300 nm ± 15, and 2) a silicon continuation etch of 200 nm to the BOX layer, followed by wet HF etching of the BOX layer.

The schematic description of the process flow is given below:

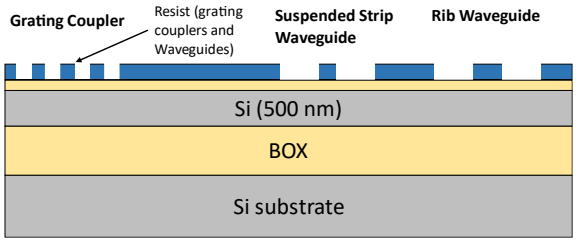
1. Starting SOI substrate



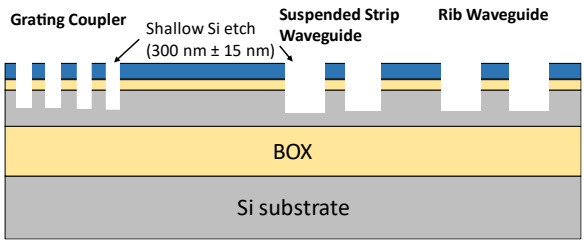
2. Hard mask (SiO_2) deposition – 200nm



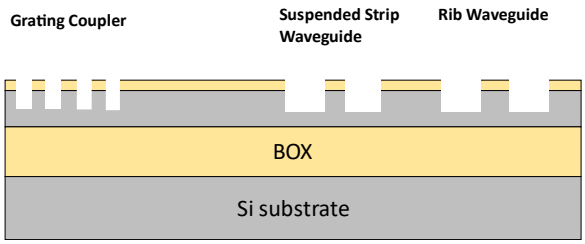
3. Resist patterning for grating couplers and waveguides – GDS layer 404



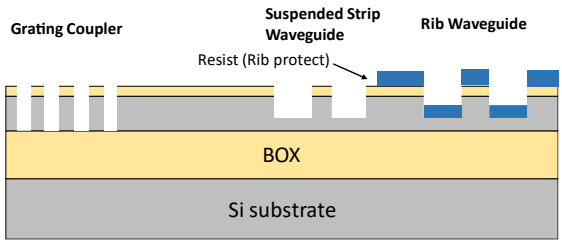
4. Hard mask etch followed by partial silicon etch (300 nm ± 15 nm)



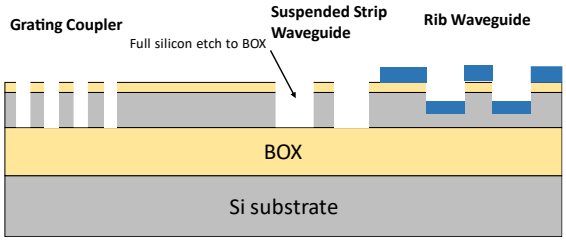
5. Resist strip



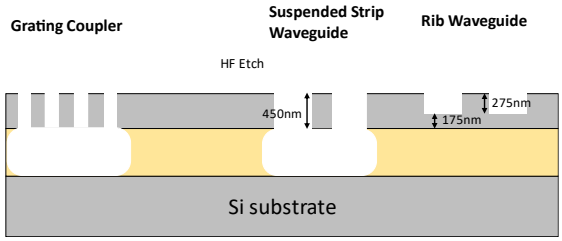
6. Resist patterning for Silicon Etch 2 (GDS layer 405) – 200 nm etch to BOX



7. Continuation Si etch (200 nm to BOX)



8. Resist strip and HF etch



During this HF etching step, the BOX is undercut by approximately 8 µm in each direction.

If you require any alternative processing steps (e.g. custom etch depths), we may be able to perform them for a small charge. Email cornerstone@soton.ac.uk with your request.

5. DESIGN RULES

It is important that designs conform to the following design rules to ensure correct processing. Please note that after HF undercut etching, **the thickness of the silicon layer reduces to 450 nm ± 20 nm** and the lateral feature size reduces by approximately 70 nm. For example, a silicon feature width of 220 nm after processing in HF reduces to 150 nm. Furthermore, the BOX is undercut by approximately 8 µm in each direction.

Users have the option to either pre-bias or not bias their design. If un-biased, the CORNERSTONE team will perform a 35 nm shrinking of all Si etched features to offset the expected etched feature size growth during HF etching. Note that the -35 nm bias is in all directions, so an etched feature becomes 70 nm narrower. Please notify the CORNERSTONE team to either BIAS/UNBIAS your designs while submitting through the online submission process outlined in Section 7.

5.1 DESIGN AREA

The standard user cell has dimensions of **11.47 x 4.9 mm²** and **5.5 x 4.9 mm²**.

5.1.1 PHYSICAL DIE SIZE

The physical size of the dies you will receive is approximately 5.3-5.6 x 12.5 mm². This area includes a border the CORNERSTONE team will add that contains alignment marks, metrology boxes etc. which surround 3x design areas from various CORNERSTONE users, as shown in Figure 1. If you require specific physical die dimensions (5.3 x 12.5 mm² or 5.6 x 12.5 mm²), for example if integration to a PCB is required, please specify the physical die dimensions you require in the online mask submission form you are required to complete as part of the submission process (see Section 8).

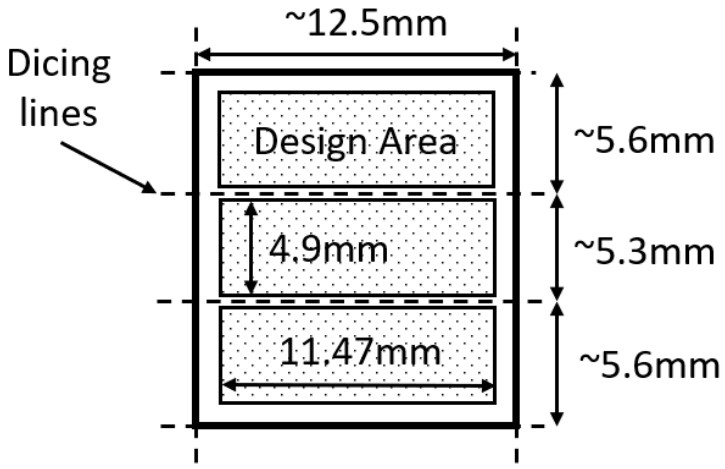


Figure 1– Physical die dimensions.

5.2 GDS LAYERS

Silicon Etch 1 (Grating couplers and waveguide) – GDS Layer 404 (Dark field) – etch depth: 300 nm ± 15 nm to BOX

This layer is used to define grating couplers as well as both suspended and rib waveguides (to form a rib waveguide, the slab region is protected during Silicon Etch 2, defined by GDS layer 405 – see below).

For users who choose to ask CORNERSTONE **'NOT TO BIAS'**: The drawn area is etched.

For users who choose to ask CORNERSTONE to **'BIAS'**: During processing, a bias of -35nm will be included in all directions to the layer 404 and the biased area is etched.

Silicon Etch 2 (Rib protect layer) – GDS Layer 405 (Light field) – etch depth: 200 nm to BOX

This layer defines the protective layer for rib waveguides. Drawn objects in this layer will be protected from etching whilst the suspended waveguides are etched to the BOX (all

areas not previously defined in the Silicon Etch 1 layer will be protected from etching by a hard mask).

Cell Outline – GDS Layer 99

This layer defines the design space boundaries (11.47 x 4.9 mm^2 or 5.5 x 4.9 mm^2).

Labels – GDS Layer 100

This layer defines text labels, which will be merged with Silicon Etch 1 (Grating coupler and Waveguides) by the CORNERSTONE team. **No islands < 20 µm are allowed.** This is because during the HF undercutting process, small features are lifted-off and may redeposit elsewhere on the wafer.

Note: You do not need to add fabrication alignment marks to your design. Layer-to-layer alignment marks will be added by the CORNERSTONE team, placed outside the design area.

5.3 MINIMUM FEATURE SIZES, TARGET CRITICAL DIMENSIONS AND OTHER DESIGN RULES

- Minimum feature sizes, minimum gaps, and maximum feature widths for each GDS layer are detailed in Table 2.
- The target critical dimension for each GDS layer is listed in Table 2. Note that other feature sizes may have a small dimensional bias.
- **No islands < 20 µm are allowed in GDS layers 404 and 100**. This is because during the HF undercutting process, small features are lifted-off and may redeposit elsewhere on the wafer.
- After HF etch, the expected lateral BOX undercut is 8 µm. Therefore, the maximum width of suspended structures should be 16 µm (see Figure 2).
- Width of the supporting structure/subwavelength structure <6 µm have proven to work (see Figure 1). **If you try more challenging dimensions, do so at your own risk.**
- A minimum spacing between waveguides of at least 75 µm is recommended to avoid suspended waveguides collapsing.
- For gaps in GDS layers 404 and 100 of less than 350 nm, limit the length to a maximum of 20 µm. This is because long, narrow resist features can collapse during resist development.
- All strip waveguides will be suspended due to the undercut etching.

5.4 DESIGN RULES SUMMARY

A summary of the design rules and GDS layer numbers described in this section is detailed in *Table 2* below.

Table 2 – Design rules summary.

Layer description	Option	GDS no.	Field	Min. feature size	Min. gap	Max. suspended waveguide width	Max. support structure width	Target critical dimension
Silicon Etch 1¥ (300 ± 15 nm)	CORNERSTONE NOT to bias	404	Dark	200 nm	250 nm	16 µm§	6 µm¤	250 nm
	CORNERSTONE to bias	404	Dark	270 nm	180 nm	16 µm§	6 µm¤	320 nm
Silicon Etch 2 (200 nm to BOX)	N/a	405	Light	200 nm	250 nm	N/a	N/a	250 nm
Cell Outline	N/a	99	N/a	N/a	N/a	N/a	N/a	N/a
Labels*¥	N/a	100	Dark	250 nm	250 nm	N/a	N/a	N/a

¥ No islands < 20 µm allowed.

§ After HF etch, the expected lateral BOX undercut is 8 µm. Therefore, the maximum width of suspended structures should be 16 µm (see Figure 2).

¤Width of the supporting structure/subwavelength structure <6 µm have proven to work (see Figure 1). **If you try more challenging dimensions, do so at your own risk.**

*Features drawn in the Labels layer will be merged into Silicon Etch 1 by the CORNERSTONE team.

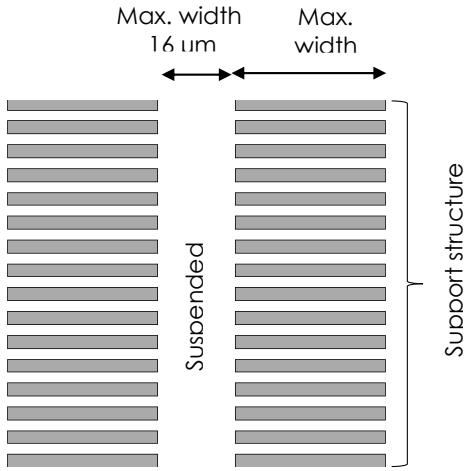


Figure 2 – Design rule for suspended and supporting/subwavelength structure maximum width.

In order to help you ensure that you comply with the design rules, you can download and execute the KLayout pre-DRC script provided by CORNERSTONE on our website www.cornerstone.sotonfab.co.uk/design-rules (note that the automatic DRC will not check all of the design rules, so it remains very important to read the design rules in detail).

For users choosing the priority option, it is essential to provide DRC-free mask layouts on or before the submission deadline. Therefore, users planning to initiate a priority batch should run the L-edit DRC file and confirm that the submitted design is free of design rule issues before the submission deadline. The CORNERSTONE team will not undertake post-submission DRC for priority access users to shorten the delivery timeline.

MPW users will have an opportunity to attend 1-to-1 Drop-in Sessions to pre-review mask layouts before the submission deadline, using this link to book a 20-mins session.

5.5 FILE FORMAT

Designs must be submitted in a Graphical Database System file (extension *.gdsII*) or Open Artwork System Interchange Standard (extension *.oas*) format. Ensure a manufacturing grid size of 1 nm is used, as per the CORNERSTONE GDSII Template file.

We recommend dedicated lithography editing software be used in the design of the *.gdsII* or *.oas* file.

5.6 GDSII TEMPLATE FILE

A *.gdsII* template file has been made available on our website containing the information described in this section. Ensure that all submitted designs fit within the specified area, and that only the designated GDS layer numbers are used.

6 QUALITY ASSESSMENT

This fabrication run will be qualified by characterising a standard test pattern that is included on the chip (not part of the user cell). The test structures that will be checked after fabrication are reported in Table 3 below, together with the values that are targeted by the CORNERSTONE platform.

Table 3 – Quality assessment parameters.

Test structure	Parameter	Value
Straight single mode suspended waveguide	Propagation loss	< 5 dB/cm for TE mode at λ = 3.8 μm

7 MASK SUBMISSION PROCEDURE

In order to be eligible to submit a design you must first sign-up to this call using the online form found using the link below. This is in order to enable us to prepare the necessary paperwork and plan the fabrication process effectively. The sign-up deadline is found at the top of this document.

www.cornerstone.sotonfab.co.uk/mpw-sign-up-form

Under no circumstances will we accept any design submissions for which we have not received a sign-up form.

After completing the sign-up form, when you are ready to submit your mask design on or before the mask submission deadline listed at the top of this document, follow the link below to the CORNERSTONE website mask submission page:

www.cornerstone.sotonfab.co.uk/gds-file-upload

A purchase order (PO) must be uploaded to this form to pay the access fee. Purchase orders will not be accepted via email. If you are accessing this call free of charge, benefitting from the CORNERSTONE 2.5 funding, simply upload a blank file.

You must also upload your design file to the submission form. Ensure that the top cell in your design file is titled 'Cell0_*[Name of Institution]*'.

For information about setting up CORNERSTONE as a supplier to your institution, or if you encounter any problems with the online forms, please contact cornerstone@soton.ac.uk.

8 MASK PROCESSING PERFORMED BY CORNERSTONE

Upon receipt of your *.gdsII* file, the CORNERSTONE team will perform the following mask processing steps in order to produce the final mask, based on the descriptions provided in Section 5.2:

Silicon Etch 1 (Waveguide layer) – GDS Layer 404 (Dark field) – etch depth: 300 nm to BOX layer:

1. (**Applicable only for 'BIAS' option**) Shrink Waveguide Etch layer (GDS layer 404) by 35 nm in all directions.
2. Merge the dark field Waveguide Etch layer (GDS layer 404) with Label layer (GDS layer 100).

Silicon Etch 2 (Rib protect layer) – GDS Layer 405 (Light field) – etch depth: 200 nm to BOX:

1. Subtract the Rib Protect layer (GDS layer 405) from the Cell Outline (GDS layer 99) to convert to a dark field mask.

9 TECHNICAL SUPPORT

If you have any questions relating to the fabrication process or design rules, please contact the CORNERSTONE team (cornerstone@soton.ac.uk).

10 CHIP DELIVERY

A total of 5 replica cells will be delivered to each user. The delivery time schedule can be found in Table 1.

11 FEEDBACK

Feedback is essential to the CORNERSTONE team. It is required to ensure a continuous improvement to the quality of our services. It is also evidence on the user satisfaction, and a measure to what extent we were able to meet user requirements. Therefore, we kindly ask our users to provide feedback to us, including device performance data, SEM images, future interests for the CORNERSTONE project etc. A feedback form will be sent to you along with your chips.

Alternatively, email cornerstone@soton.ac.uk with your comments.

12 PUBLICATIONS

If you are benefitting from free-of-charge access via the CORNERSTONE 2.5 funding, please include the following statement in the "Funding" section of any publications:

"The chip fabrication for this research was funded by the Engineering and Physical Sciences Research Council (EPSRC) CORNERSTONE 2.5 (EP/W035995/1) project."

If you are benefitting from subsidised access via the C-PIC funding, please include the following statement in the "Funding" section of any publications:

"The chip fabrication for this research was funded by the Engineering and Physical Sciences Research Council (EPSRC) C-PIC (EP/Z531066/1) project."

This is important to us to be able to demonstrate impact from the funding.

If you are a paying user, we kindly ask that you include CORNERSTONE in the "Acknowledgments" section of any publications that result from the chips you receive from CORNERSTONE.