CORNERSTONE DESIGN GUIDELINES
220 nm SOI Active MPW #43 March 2025

SIGN-UP DEADLINE: 16/04/2025
MASK SUBMISSION DEADLINES: 14/05/2025(SOFT) AND 28/05/2025(HARD)

1 TERMS AND CONDITIONS AND COST

All design submissions must agree with the terms and conditions:

www.cornerstone.sotonfab.co.uk/terms-and-conditions

Under no circumstances will we accept designs without agreement with the terms.

Therefore, we strongly recommend that the terms and conditions are pre-authorised by your institution prior to the mask submission date.

A purchase order (PO) must be uploaded at the same time as submitting your mask design in order pay the access fee, detailed in Table 1 below. Purchase orders will not be accepted via email.

Table 1 – Access cost and Delivery Time.

Design Area [mm²]	11.47 x 4.9	5.5 x 4.9	Delivery Time
Access Cost * (Standard)	£48,750	£29,250	36 weeks
Access Cost for Enterprises and Academia based in UK†	50% off	50% off	36 weeks

*Quoted prices are exclusive of VAT, import duties/customs fees, withholding taxes etc.

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†**Are you a UK company or academic?**

UK companies and universities may be eligible for a 50% discount on the cost of this MPW run with support from the CORNERSTONE Photonics Innovation Centre (C-PIC) (EP/Z531066/1), funded by UK Research and Innovation. Support will be provided under the Subsidy Control Act (2022) via Minimal Financial Assistance. To be eligible you will need to demonstrate the potential impact of receiving assistance against one or more of the following categories: impact on jobs and skills, access to new technology, accelerating product development. Following submission of your sign-up form, you will receive correspondence with more details of how this support will be provided. The support is only available to UK companies using CORNERSTONE for prototyping and product development.

To receive Design Rule Check (DRC) feedback from the CORNERSTONE team, users must submit their designs no later than the soft deadline. A two-week DRC window for re-submissions will then be available to those who submit their designs before the soft deadline. Submissions received after the soft deadline will not be checked against design rules; therefore, any fabrication failures related to design rule violations will be at the users' own risk. Submissions received after the hard deadline will not be accepted under any circumstances.

For information about setting up CORNERSTONE as a supplier to your institution, please contact cornerstone@soton.ac.uk.

2 DESIGN RULE CHANGES FROM PREVIOUS CALL (MPW #38)

- Minimum gap rule in layer 13 reduced from 4 µm to 2 µm

3 IPKISS PROCESS DESIGN KIT

For the greatest functionality, we recommend that you use Luceda's IPKISS software to access the process design kit (PDK), after purchasing the required license. The IPKISS platform enables the automation and integration of all aspects of your photonic design flow in one tool, using one standard language. The PDK can be used in either IPKISS' Python coding environment or in the GUI of Siemens EDA L-Edit by using the IPKISS Link for Siemens EDA.

To obtain a copy of the software and a license key, please contact Luceda by sending an email to info@lucedaphotonics.com, specifying that you require a license for CORNERSTONE PDK usage. Luceda will contact you within 1-2 working days following the receipt of your request to provide a quote for the license. Of course, if you already have a valid license, the PDK can be accessed free of charge.

For more information, please visit www.lucedaphotonics.com.

Once you have access to the Luceda software, in order to obtain a copy of the CORNERSTONE PDK, please contact Luceda support at info@lucedaphotonics.com. An account will be created for you at support.lucedaphotonics.com for any technical support on Luceda's IPKISS software or the CORNERSTONE PDK implementation.

We also have a PDK available for download in .gdsII format.

4 PROCESS FLOW

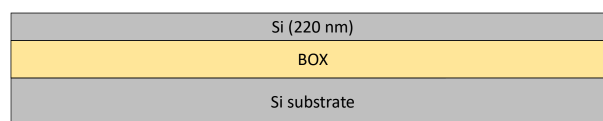
For this call, the patterns will be processed on a single-side polished Silicon-on-Insulator (SOI) wafer, with the following nominal parameters:

- Crystalline silicon (Si) substrate with the resistivity of 750 Ω.cm
- Thermal silica (SiO_2) Buried OXide (BOX) layer with a thickness h_{box} = 2 µm
- Crystalline silicon (Si) core layer (100)-oriented with a thickness h_{wg}=220 nm ± 20 nm

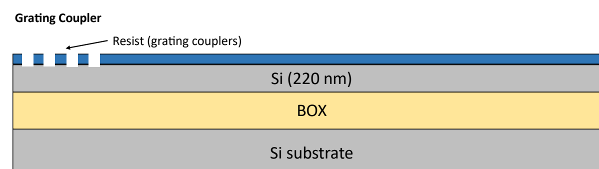
We will offer three silicon etch processes: 1) a shallow silicon etch of 70 nm ± 10 nm, 2) an intermediate silicon etch of 120 nm ± 10 nm, and 3) a continuation silicon etch of a further 100 nm to the BOX layer. We will offer four silicon implantation steps: 1) a low dose p-type implant, 2) low dose n-type implants, 3) a high dose p-type implant for ohmic contacts, and 4) a high dose n-type implant for ohmic contacts. More information on the implant conditions can be found in Section 4.1. We will offer a single metal layer for ohmic silicon contacts, on top of a 1 µm ± 100 nm thick silicon dioxide top cladding layer. Heaters can be included in this metal electrode layer. Also, we offer a Silicon implant window for defect detectors.

The schematic description of the process flow is given below.

1. Starting SOI substrate



2. Resist patterning for Silicon Etch 1 (GDS layer 6) – 70 nm ± 10 nm etch



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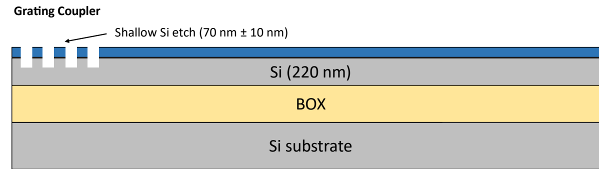
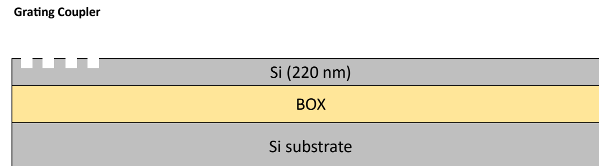
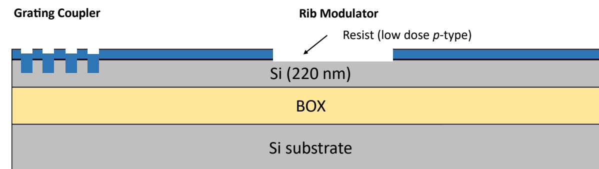
3. Shallow Si etch (70 nm ± 10 nm etch depth)



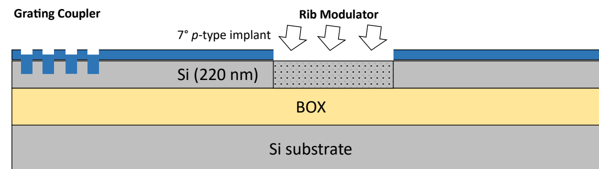
4. Resist strip



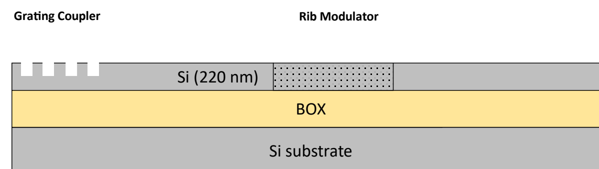
5. Resist patterning for Low Dose p-type Implant (GDS layer 7)



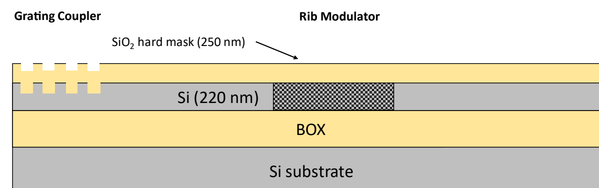
6. Low dose p-type implant (7°)



7. Resist strip



8. Silicon dioxide hard mask deposition – 180 nm



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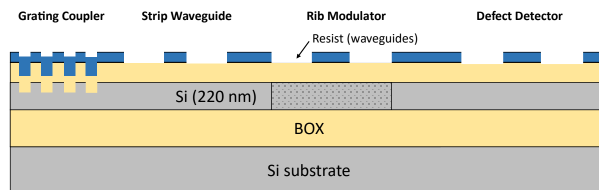
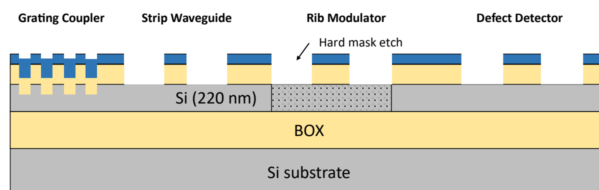
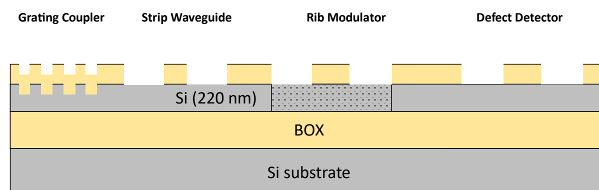
9. Resist patterning for Silicon Etch 2 (GDS layers 3 & 4) – 120 nm ± 10 nm etch



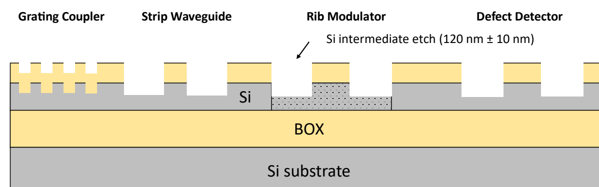
10. Hard mask etch



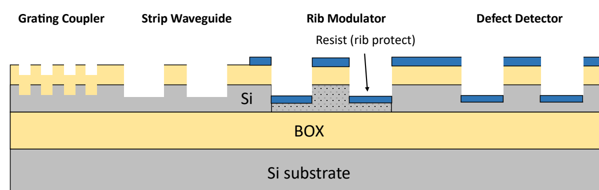
11. Resist strip



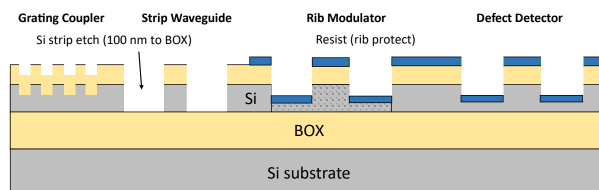
12. Intermediate Si etch (120 nm ± 10 nm etch depth)



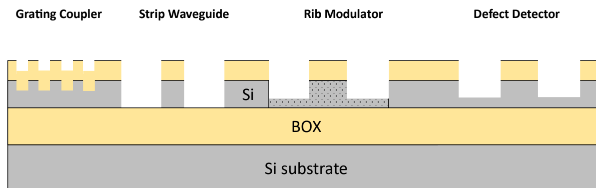
13. Resist patterning for Silicon Etch 3 (GDS layer 5) – 100 nm etch to BOX



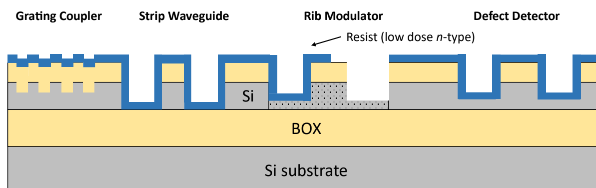
14. Si continuation etch to BOX (100 nm etch to BOX)



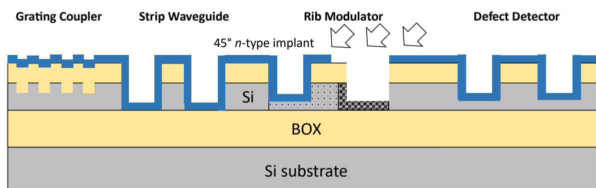
15. Resist strip



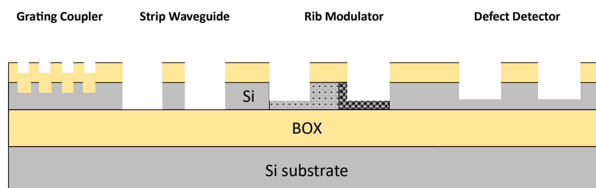
16. Resist patterning for Low Dose n-type Implant (GDS layer 8)



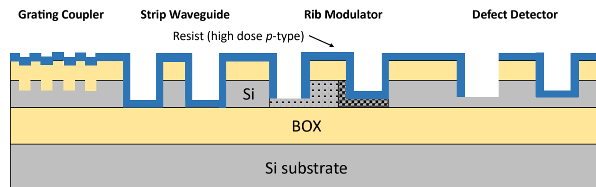
17. Angled low dose n-type implant (45°) - x6 with 60° wafer rotation between each implant



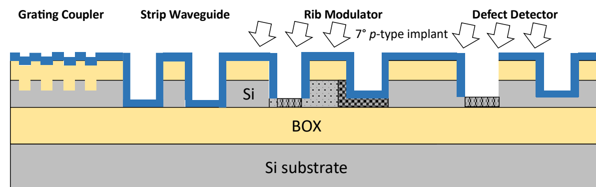
18. Resist strip



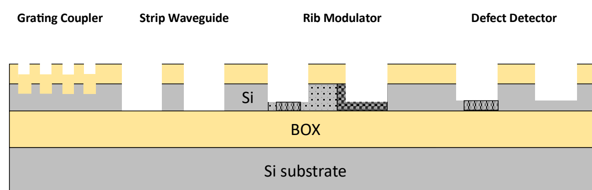
19. Resist patterning for High Dose p-type Implant (GDS layer 9)



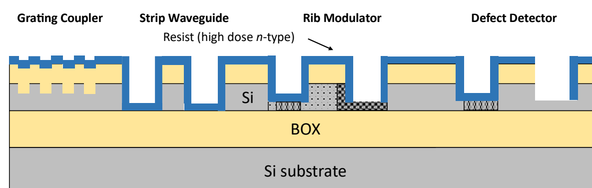
20. High dose p-type implant (7°)



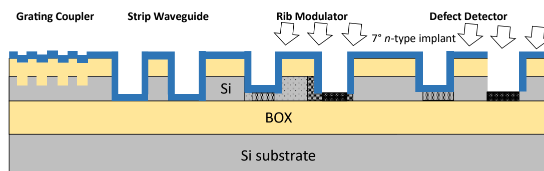
21. Resist strip



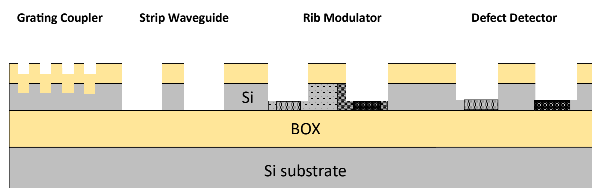
22. Resist patterning for High Dose n-type Implant (GDS layer 11)



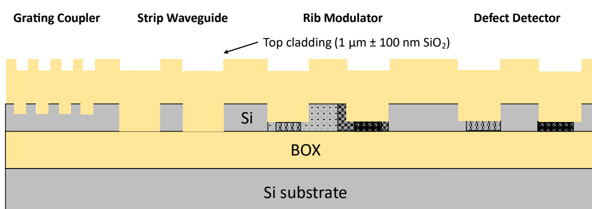
23. High dose n-type implant (7°)



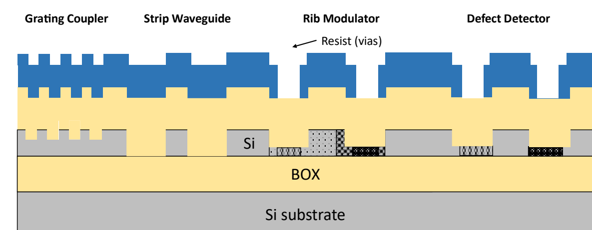
24. Resist strip and dopant activation



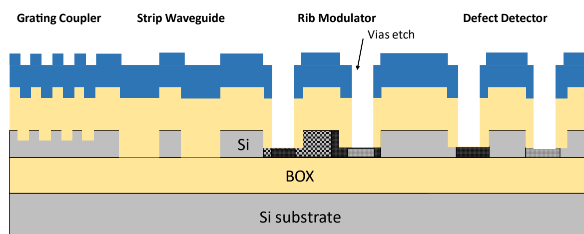
25. Deposition of 1 µm ± 100 nm thick SiO_2 top cladding



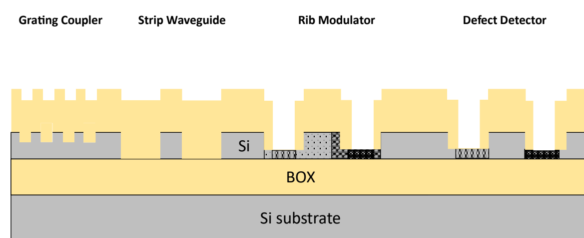
26. Resist patterning for Vias (GDS layer 12)



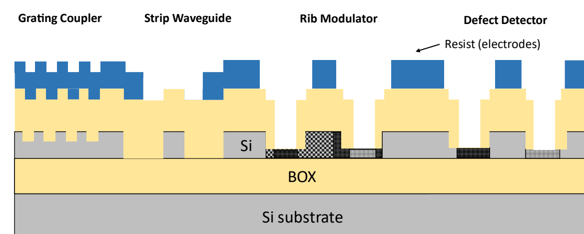
27. SiO_2 vias etch



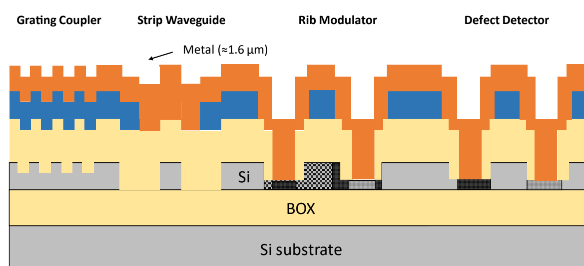
28. Resist strip



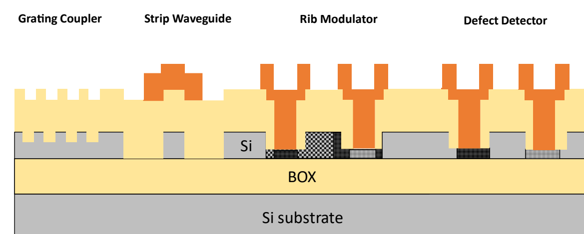
29. Resist patterning for Electrodes (GDS layer 13)



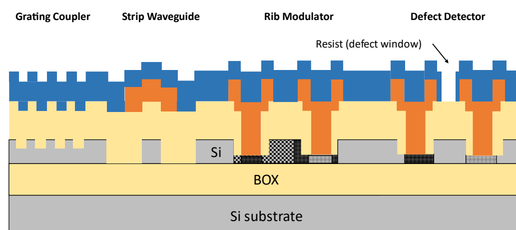
30. Metal stack deposition ≈ 1.6 µm



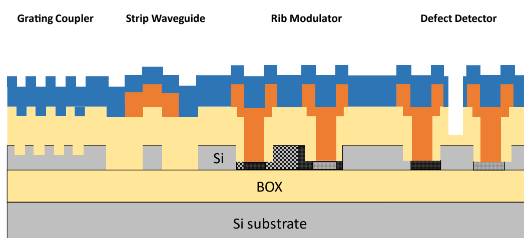
31. Metal lift-off



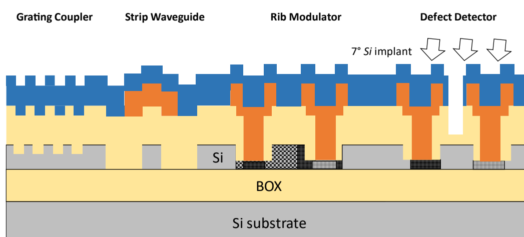
32. Resist patterning for Si Implantation window (GDS layer 23)



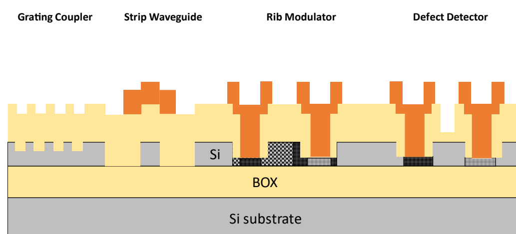
33. Oxide etch with 200nm footing thickness for Si implantation window



34. Si Implantation for defect detector formation



35. Resist Strip and anneal



If you require any alternative processing steps (e.g. custom etch depths), we may be able to perform them for a suitable charge. Email cornerstone@soton.ac.uk with your request.

4.1 PROCESS PARAMETERS OVERVIEW

A cross-section of a carrier depletion modulator structure is shown in Figure 1, along with the important device parameters, including doping concentrations, listed in Table 2.

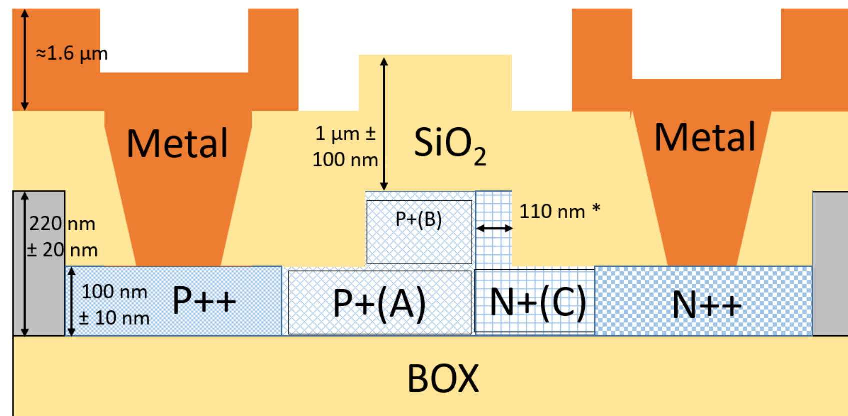


Figure 1 – *Process parameters overview. *The N+ implant is performed at 45°, so the implanted region is fixed at 110 nm from waveguide edge (controlled by the angled implant energy).*

Table 2 – Important device parameters.

Property	Specification
Si overlayer thickness	220 nm ± 20 nm
Grating etch depth	70 nm ± 10 nm
Rib waveguide etch depth	120 nm ± 10 nm
P+ region (A)	≈ 5.7E17 cm^{-3}
P+ region (B)	≈ 2.25E17 cm^{-3}
N+ region (C)*	≈ 1.1E18 cm^{-3}
P++	≈ 1E20 cm^{-3}
N++	≈ 1E20 cm^{-3}
Top cladding SiO_2 thickness	1 µm ± 100 nm
Metal thickness	≈ 1.6 µm

**Note:* The low dose *n*-type implant concentrations are compensated by the background low dose *p*-type implant (i.e. the low dose *n*-type region must fully overlap with the low dose p-type region; otherwise, the actual *n*-type concentrations will be higher than specified).

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If alternative implant conditions are required, we may be able to perform them for a suitable charge. Email cornerstone@soton.ac.uk with your request.

5 DESIGN RULES

It is important that designs conform to the following design rules to ensure clarity and correct processing.

5.1 DESIGN AREA

The standard user cell has dimensions of **11.47 x 4.9 mm²** and **5.5 x 4.9 mm²**

5.1.1 PHYSICAL DIE SIZE

The physical size of the dies you will receive is approximately 5.3-5.6 x 12.5 mm². This area includes a border the CORNERSTONE team will add that contains alignment marks, metrology boxes etc. which surround 3x design areas from various CORNERSTONE users, as shown in Figure 2. If you require specific physical die dimensions (5.3 x 12.5 mm² or 5.6 x 12.5 mm²), for example if integration to a PCB is required, please specify the physical die dimensions you require in the online mask submission form you are required to complete as part of the submission process (see Section 8).

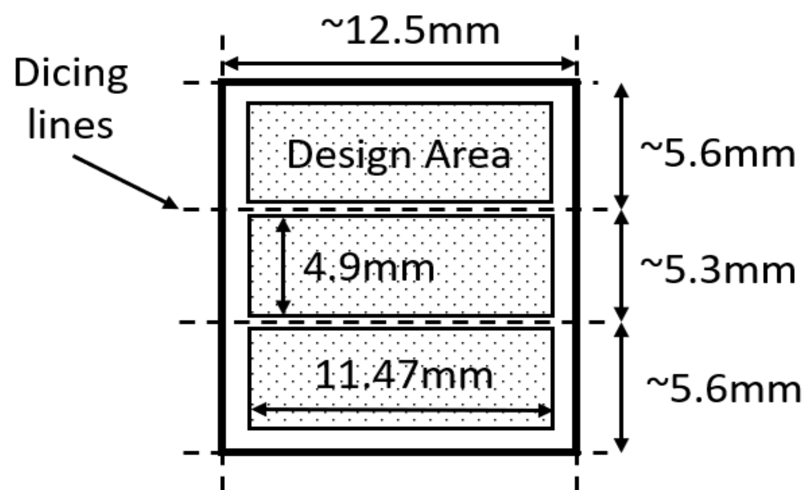

Figure 2 - *Physical die dimensions.*

5.2 GDS LAYERS

Each lithographic step in the fabrication process flow is identified by a specific GDS layer/s. These are as follows:

Silicon Etch 1 (Grating couplers) – GDS Layer 6 (Dark field) – etch depth: 70 nm ± 10 nm

This layer is used to define grating couplers, which are fabricated with 70 nm shallow silicon etching. The drawn area is etched.

Silicon Etch 2 (Waveguide layer) – GDS Layer 3 (Light field) & GDS Layer 4 (Dark field) – etch depth: 120 nm ± 10 nm

This layer defines both strip and rib waveguides (to form a rib waveguide, the slab region is protected during Silicon Etch 3, defined by GDS layer 5 – see below), and is split into two separate GDS layer numbers, patterned into the same resist and etched together:

GDS Layer 3: Drawn objects on this layer will be protected from the silicon etch. Users should draw the waveguides and any other features to remain following 120 nm silicon etching (to the rib waveguide height). During fracturing processing, this will be translated into a pattern that defines 5 µm wide trenches on either side of the waveguides drawn in GDS layer 3 (see Figure 3).

Figure 3 - Description of GDS Layer 3 processing.

If you require waveguide trenches that are a different width, refer to the guidelines for generating the trenches in Section 9. You can complete these steps yourself and modify the growth function dimension in step 1.

GDS Layer 4: Drawn objects on this layer will be exposed to the 120 nm silicon etch (to the rib waveguide height). An example photonic crystal structure is shown in Figure 4. The important thing to note here is that the waveguide layer drawn in GDS layer 3 should overlap the structures drawn in GDS layer 4, so that when the 5 µm trenches are generated by CORNERSTONE, a continuous waveguide remains.

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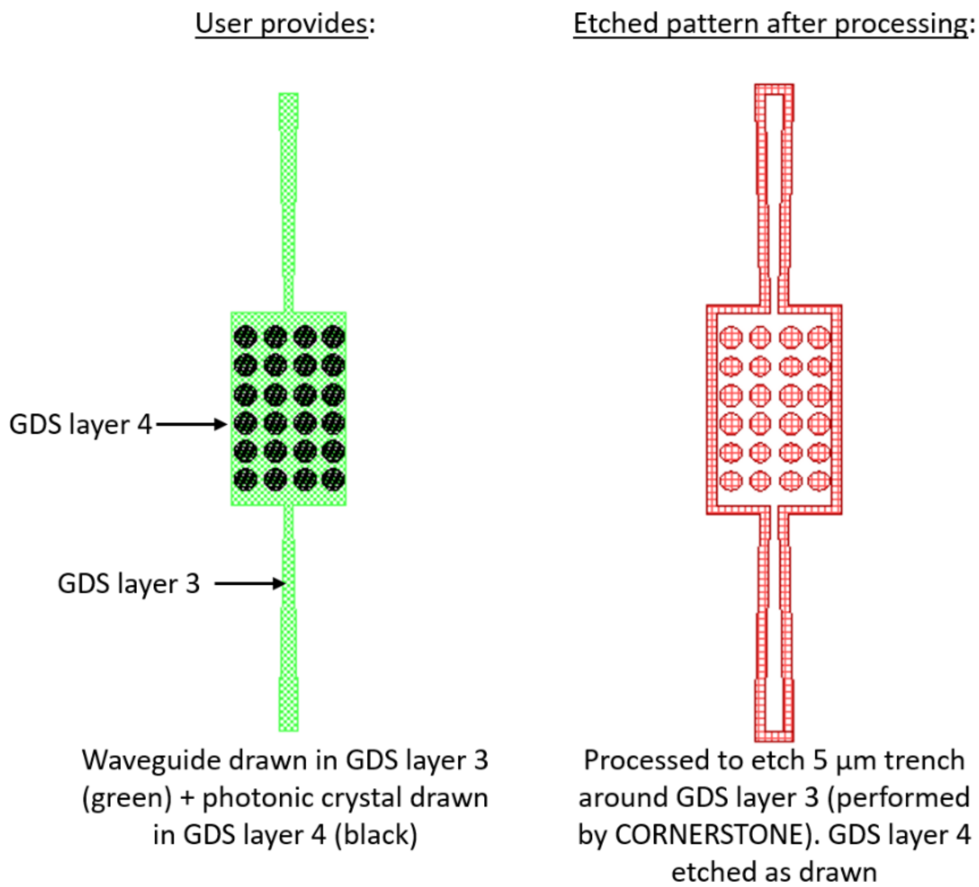

Figure 4 – Example photonic crystal structure using GDS Layers 3 & 4.

Silicon Etch 3 (Rib protect layer) – GDS Layer 5 (Light field) – etch depth: 100 nm to BOX

This layer defines the protective layer for rib waveguides. Drawn objects in this layer will be protected from etching whilst the strip waveguides are etched to the BOX (all areas not previously defined in the Silicon Etch 2 layer will be protected from etching by a hard mask). We recommend that this layer should extend more than or equal to 5 µm from the edge of features drawn in GDS layer 3 so that the 5 µm wide trenches etched in the previous partial silicon etching step are fully protected by GDS layer 5, with the exception of any rib-to-strip transitions. An overview of how to draw both strip and rib waveguides is shown in Figure 5.

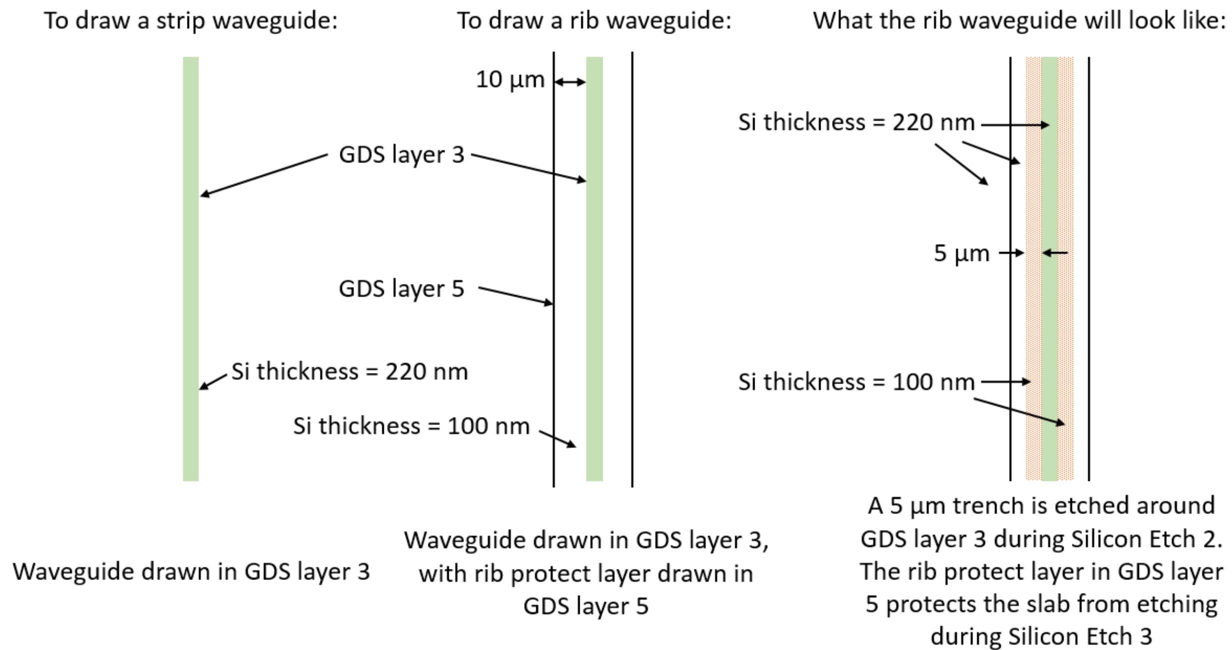

Figure 5 – Drawing strip and rib waveguides.

Low dose p-type Implant – GDS Layer 7 (Dark field)

This layer defines the background low dose *p*-type implant. Drawn objects in this layer will be implanted. The approximate doping concentration levels are detailed in Table 2 in Section 4.1 above.

Low dose n-type Implant – GDS Layer 8 (Dark field)

This layer defines the low dose *n*-type implant. Drawn objects in this layer will be implanted. The approximate doping concentration levels are detailed in in Table 2 in Section 4.1 above. In order for the listed doping concentrations to be valid, the low dose *n*-type region must fully overlap with the low dose *p*-type region. Otherwise, the actual *n*-type concentrations will be higher than specified.

A self-aligned process is used for the low dose *n*-type implant (i.e. the waveguides are etched through an oxide hard mask, and the low dose *n*-type implant is performed with hard mask still in place). Therefore, no matter where the low dose *n*-type edge is drawn within the waveguide, it will be masked from above the waveguide by the hard mask. The implant depth into the waveguide sidewall (45° angled implant) is approximately 110 nm, and is controlled by the implant energy. Therefore, it is best to position the low dose *n*-type implant boundary in the centre of the waveguide to remove any alignment error.

In order to enable any waveguide sidewall to be implanted independently of the waveguide orientation, six identical implants will be performed on the wafer with a 60° wafer rotation between each implant.

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High dose p-type Implant – GDS Layer 9 (Dark field)

This layer defines the high dose *p*-type implant for ohmic Si contacts. Drawn objects in this layer will be implanted. The approximate doping concentration levels are detailed in Table 2 in Section 4.1 above. Implants in this layer will be into the slab region of the waveguide (100 nm Si thickness) i.e. this layer will be merged with the Silicon Etch 2 (Waveguides) and Silicon Etch 3 (Rib protect) layers by CORNERSTONE, as shown in Figure 6 and detailed in Section 9.

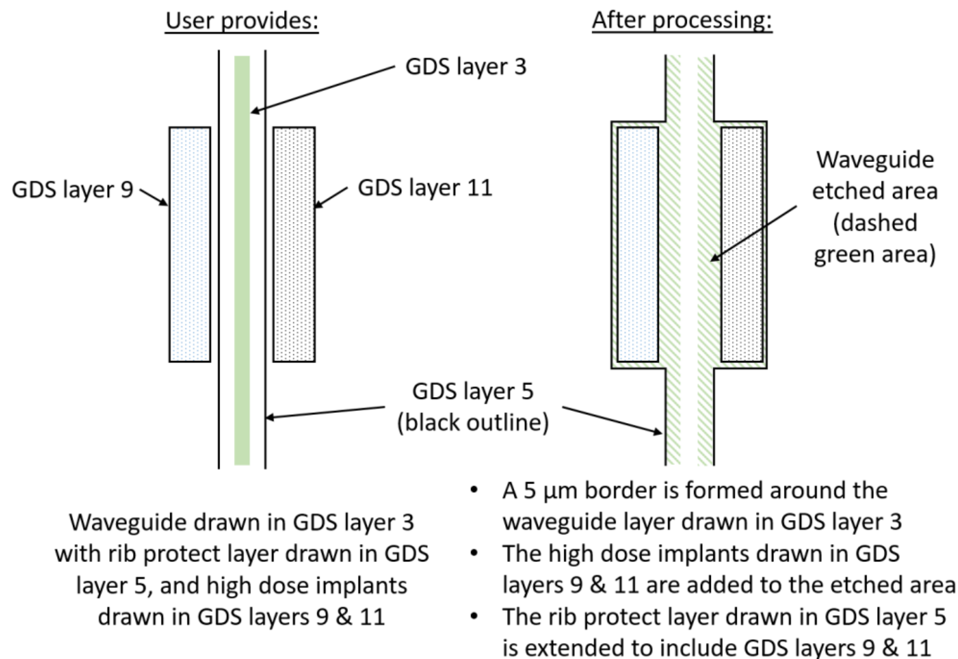

Figure 6 – Processing of high dose implant areas.

High dose n-type Implant – GDS Layer 11 (Dark field)

This layer defines the high dose *n*-type implant for ohmic Si contacts. Drawn objects in this layer will be implanted. The approximate doping concentration levels are detailed in Table 2 in Section 4.1 above. Implants in this layer will be into the slab region of the waveguide (100 nm Si thickness) i.e. this layer will be merged with the Silicon Etch 2 (Waveguides) and Silicon Etch 3 (Rib protect) layers by CORNERSTONE, as shown in Figure 6 and detailed in Section 9.

Vias – GDS Layer 12 (Dark field)

This layer defines the vias in the 1 µm thick SiO_2 top cladding layer for ohmic Si contacts. Drawn objects in this layer will be etched. All structures drawn in this layer must be inclusive of either the High Dose *p*-type Implant (GDS layer 9) or the High Dose *n*-type Implant (GDS layer 11) by at least 500 nm as shown in Figure 7 (i.e. the high dose implant layer must extend in all directions at least 500 nm beyond the vias layer).

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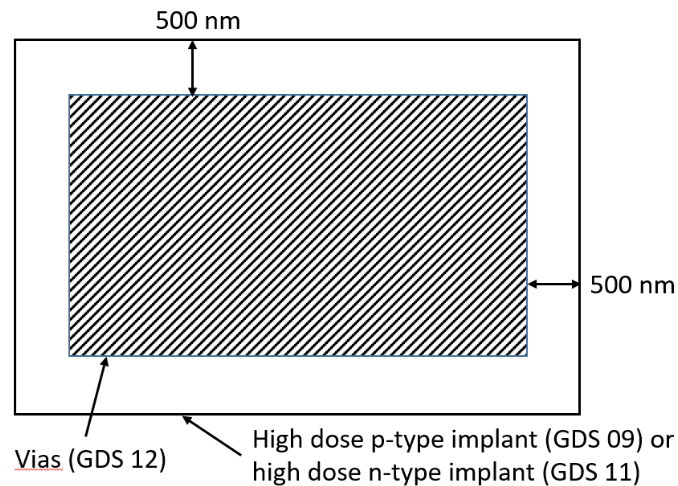

Figure 7 – Vias layer inclusive of high dose implant layers.

Electrodes – GDS Layer 13 (Light field)

This layer defines the metal electrodes. Drawn objects on this layer will remain after metal lift-off. Heaters can also be defined in this layer. All structures drawn in the Vias layer (GDS layer 12) must be inclusive of the metal contacts drawn in the Electrodes layer (GDS layer 13) by at least 500 nm as shown in Figure 8 (i.e. the electrode layer must extend in all directions at least 500 nm beyond the vias layer).

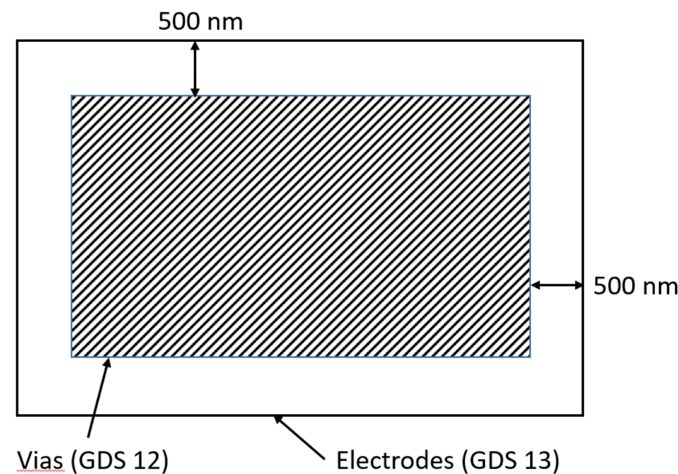

Figure 8 – Vias layer inclusive of electrodes layers.

Defect Detector – GDS 23

This layer defines the Si implantation window for the formation of defect-based detectors. Drawn objects in this layer will be etched and therefore implanted. The top oxide cladding is etched 200 nm above the waveguide for opening an implantation window. Features drawn in this layer should have a minimum of 5 μm gap between features drawn in GDS layer 13 (Electrodes).

Cell Outline – GDS Layer 99

This layer defines the design space boundaries (11.47 x 4.9 mm^2, 5.5 x 4.9 mm^2, 2.5 x 4.9 mm^2 and 2.5 x 2.5 mm^2).

Labels – GDS Layer 100

This layer defines text labels, which will be merged with Silicon Etch 2 (Waveguides) by the CORNERSTONE team. This layer will not have any design rule checking (DRC) performed.

Note: You do not need to add fabrication alignment marks to your design. Layer-to-layer alignment marks will be added by the CORNERSTONE team, placed outside the design area.

5.3 MINIMUM FEATURE SIZES, TARGET CRITICAL DIMENSIONS AND OTHER DESIGN RULES

- Minimum feature sizes, minimum gaps, and maximum feature widths for each GDS layer are detailed in Table 3.
- The target critical dimension for each GDS layer is listed in Table 3. Note that other feature sizes may have a small dimension bias.
- A minimum spacing between waveguides of at least 5 µm is recommended to avoid power coupling.
- An overlap of at least 200 nm between GDS layers is essential to account for the alignment tolerance between layers.
- All structures drawn in GDS layer 6 (Grating couplers) must overlap by at least 200 nm with GDS layer 3 (Waveguides).
- All structures drawn in GDS layer 9 and GDS layer 11 (high dose implant layers) should not overlap with GDS layer 3 (Waveguides). The high dose implants will be masked by the hard mask regardless.
- All structures drawn in GDS layer 12 (Vias) must be inclusive of either GDS layer 9 (High Dose *p*-type Implant) or GDS layer 11 (High Dose *n*-type Implant) by at least 500 nm (i.e. the high dose implant layer must extend in all directions at least 500 nm beyond the vias layer).
- All structures drawn in GDS layer 12 (Vias) must be inclusive of the metal contacts drawn in GDS layer 13 (Electrodes) by at least 500 nm (i.e. the electrode layer must extend in all directions at least 500 nm beyond the vias layer).
- Ensure all structures drawn in GDS layer 6 (Grating couplers) do not overlap with either GDS layer 12 (Vias) or GDS 13 (Electrodes).
- Defect detector layer (GDS 23) should not overlap with Metal or Vias layers.
- Spacing between GDS layer 23 and GDS layer 13 should be at least 5 µm.

5.4 DESIGN RULES SUMMARY

A summary of the design rules and GDS layer numbers described in this section is detailed in Table 3 below.

Table 3 – Design rules summary.

Layer description	GDS number	Field	Min. feature size	Min. gap	Max. feature width
Silicon Etch 1 (70 nm ± 10 nm)	6	Dark	200 nm	250 nm	20 µm
			200 nm	350 nm	N/a
Silicon Etch 2 (120 nm ± 10 nm)	3	Light	350 nm	200 nm	N/a
	4	Dark	200 nm	350 nm	
Silicon Etch 3 (100 nm to BOX)	5	Light	250 nm	250 nm	N/a
Low Dose *p*-type Implant	7	Dark	500 nm	500 nm	N/a
Low Dose *n*-type Implant*	8	Dark	500 nm	500 nm	N/a
High Dose *p*-type Implant	9	Dark	500 nm	500 nm	N/a
High Dose *n*-type Implant	11	Dark	500 nm	500 nm	N/a
Vias	12	Dark	3 µm	5 µm	N/a
Electrodes	13	Light	6 µm	2 µm	N/a
Defect detector implant	23	Dark	5 µm	5 µm	N/a
Cell Outline	99	N/a	N/a	N/a	N/a
Labels**	100	Dark	250 nm	250 nm	N/a

*45° angled implant at 6x wafer rotations (separated by 60° rotation).
**Features drawn in the Labels layer will be merged into Silicon Etch 2 by the CORNERSTONE team.

In order to help you ensure that you comply with the design rules, you can download and execute the KLayout pre-DRC script provided by CORNERSTONE on our website www.cornerstone.sotonfab.co.uk/design-rules (note that the automatic DRC will not check all of the design rules, so it remains very important to read the design rules in detail).

MPW users will have an opportunity to attend 1-to-1 Drop-in Session to pre-review mask layouts before the submission deadline, using the link to book a 20-min session.

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5.5 FILE FORMAT

Designs must be submitted in a Graphical Database System file (extension *.gdsII*) or Open Artwork System Interchange Standard (extension *.oas*) format. Ensure a manufacturing grid size of 1 nm is used, as per the CORNERSTONE GDSII Template file.

We recommend dedicated lithography editing software be used in the design of the *.gdsII* or *.oas* file.

5.6 GDSII TEMPLATE FILE

A *.gdsII* template file has been made available on our website containing the information described in this section. Ensure that all submitted designs fit within the specified area, and that only the designated GDS layer numbers are used.

6 MATERIAL PROPERTIES

The measured refractive indices of Silicon and SiO_2 layers are shown in Figure 9 below. This data is also available in tabular format on our website.

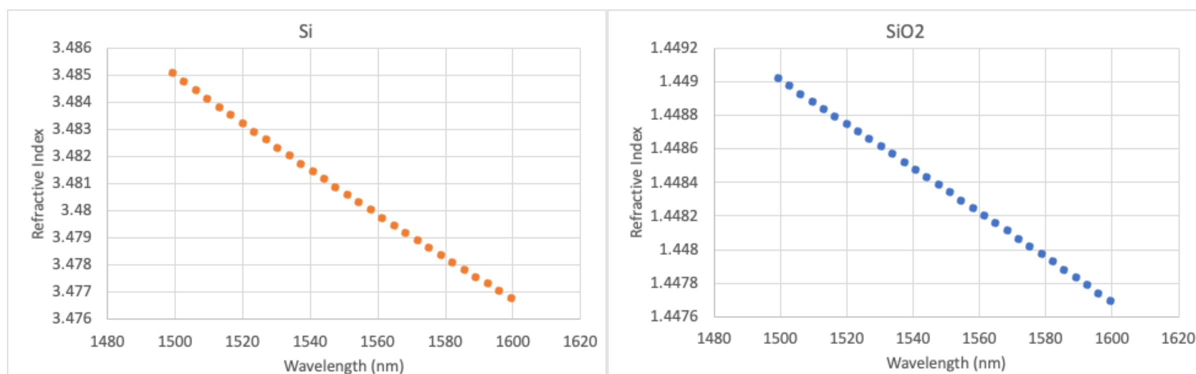

Figure 9 – *Refractive indices of Silicon (left) and* SiO_2 (right).

7 QUALITY ASSESSMENT

This fabrication run will be qualified by characterising a standard test pattern that is included on the chip (not part of the user cell). The test structures that will be checked after fabrication are reported in Table 4, together with the values that are targeted by the CORNERSTONE platform.

Table 4 – Quality assessment parameters.

Test structure	Parameter	Value
Straight single mode rib waveguide	Propagation loss	< 4 dB/cm for TE mode
1.8 mm long MZI based carrier depletion modulator	Speed @ 2 V dual drive	28 Gb/s
	Insertion loss @ 2 V dual drive	< 5 dB
	Extinction ratio @ 2 V dual drive	> 3 dB

8 MASK SUBMISSION PROCEDURE

In order to be eligible to submit a design you must first sign-up to this call using the online form found using the link below. This is in order to enable us to prepare the necessary paperwork and plan the fabrication process effectively. The sign-up deadline is found at the top of this document.

www.cornerstone.sotonfab.co.uk/home/mpw-sign-up-form

Under no circumstances will we accept any design submissions for which we have not received a sign-up form.

After completing the sign-up form, when you are ready to submit your mask design on or before the mask submission deadline listed at the top of this document, follow the link below to the CORNERSTONE website mask submission page:

www.cornerstone.sotonfab.co.uk/gds-file-upload

A purchase order (PO) must be uploaded to this form to pay the access fee. Purchase orders will not be accepted via email.

After completion of the mask submission form, you will be emailed instructions on how to share your design file with the CORNERSTONE team. Ensure that the top cell in your design file is titled ‘Cell0_*[Name of Institution]*’.

For information about setting up CORNERSTONE as a supplier to your institution, please contact cornerstone@soton.ac.uk.

9 MASK PROCESSING PERFORMED BY CORNERSTONE

Upon receipt of your *.gdsII* file, the CORNERSTONE team will perform the following mask processing steps in order to produce the final mask, based on the descriptions provided in Section 5.2.

Silicon Etch 2 (Waveguide layer) – GDS Layer 3 (Light field) & GDS Layer 4 (Dark field) – etch depth: 120 nm ± 10 nm:

1. Grow Waveguide layer (GDS layer 3) by 5 µm in all directions.
2. Grow high dose implant layers (GDS layer 9 and GDS layer 11) by 200 nm in all directions.
3. Merge the outputs of (1) and (2).
4. Subtract the Waveguide layer (GDS layer 3) from the output of (3) to produce the etch trenches around the drawn waveguides, incorporating the high dose implant layers.
5. Merge the output of (4) with the dark field Waveguide Etch layer (GDS layer 4) and the Labels layer (GDS layer 100).

Silicon Etch 3 (Rib protect layer) – GDS Layer 5 (Light field) – etch depth: 100 nm to BOX:

1. Grow high dose implant layers (GDS layer 9 and GDS layer 11) by 300 nm in all directions.
2. Merge the output of (1) with the Rib Protect layer (GDS layer 5).
3. Subtract the output of (2) from the Cell Outline (GDS layer 99) to convert to a dark field mask.

Vias – GDS Layer 12 (Dark field)

1. Shrink high dose implant layers (GDS layer 9 and GDS layer 11) and electrodes layer (GDS layer 13) by 500 nm in all directions.
2. Perform AND function between Vias layer (GDS layer 12) and output of (1).

10 TECHNICAL SUPPORT

If you have any questions relating to the fabrication process or design rules, please contact the CORNERSTONE team (cornerstone@soton.ac.uk).

11 DEVICE DELIVERY

A total of 10 replica cells will be delivered to each user. The delivery time schedule can be found in Table 1.

12 FEEDBACK

Feedback is essential to the CORNERSTONE team. It is required to ensure a continuous improvement to the quality of our services. It is also evidence on the user satisfaction, and a measure to what extent we were able to meet user requirements. Therefore, we kindly ask our users to provide feedback to us, including device performance data, SEM

images, future interests for the CORNERSTONE project etc. A feedback form will be sent to you along with your chips.

Alternatively, email cornerstone@soton.ac.uk with your comments.

13 PUBLICATIONS

If you are benefitting from subsidised access via the C-PIC funding, please include the following statement in the "Funding" section of any publications:

"The chip fabrication for this research was funded by the Engineering and Physical Sciences Research Council (EPSRC) C-PIC (EP/Z531066/1) project."

This is important to us to be able to demonstrate impact from the funding.

If you are a paying user, we kindly ask that you include CORNERSTONE in the "Acknowledgments" section of any publications that result from the chips you receive from CORNERSTONE.

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