# DESIGN GUIDELINES FOR UNIVERSITY OF SOUTHAMPTON SILICON PHOTONICS DEVICE FABRICATION

## 220 nm SOI Passive MPW #8 for Academia

**SIGN UP DEADLINE:** 11/02/2026
**DESIGN SUBMISSION DEADLINE:** 25/03/2026
All deadlines end at 13:00 (UK time)

## 1 TERMS AND CONDITIONS AND COST

All design submissions must agree with the terms and conditions:

www.cornerstone.sotonfab.co.uk/terms-and-conditions

Under no circumstances will we accept designs without agreement with the terms.

Therefore, we strongly recommend that the terms and conditions are pre-authorised by your institution prior to the mask submission date.

Access to fabrication batch is exclusively limited to undergraduate (BSc and MSc) and 1st year postgraduate (PhD) students. Students are advised that they will be provided with a 25 x 33 mm² chip, which will include their individual designs, the contributions of other project partners, and a schematic to clearly identify the location of their specific design.

A purchase order (PO) must be uploaded at the same time as submitting your mask design in order pay the access fee, detailed in Table 1 below. Purchase orders will not be accepted via email.

*Table 1 – Access cost and Delivery Time.*

| Design Area [mm²] | 6 x 3 |
|---|---|
| Access Cost* | £100 |

*Quoted prices are exclusive of VAT, import duties/customs fees, withholding taxes, and a £25 shipping cost. The shipping cost will be charged only once per batch.

## 2 FILE FORMAT

Designs must be submitted in a Graphical Database System file format (extension *.gdsII*). Ensure a manufacturing grid size of 1 nm is used, as per the design template. We recommend dedicated lithography editing software be used in the design of the *.gdsII* file.

## 3 PROCESS FLOW

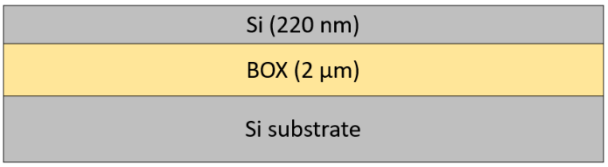
Designs will be processed on a single-side polished Silicon-on-Insulator (SOI) wafer, with the following nominal parameters:

- Crystalline silicon (Si) substrate
- Thermal silica ($SiO_2$) Buried OXide (BOX) layer with a thickness $h_{box}$ = 2 µm ± 50 nm
- Crystalline silicon (Si) core layer (100)-oriented with a thickness $h_{wg}$ = 220 nm ± 20 nm

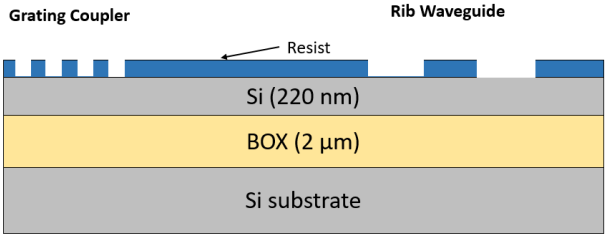
We offer a single silicon etch of 120 nm ± 10 nm. We will deposit a 1 µm ± 100 nm thick silicon dioxide top cladding layer after silicon etching.

The schematic description of the process flow is given below:

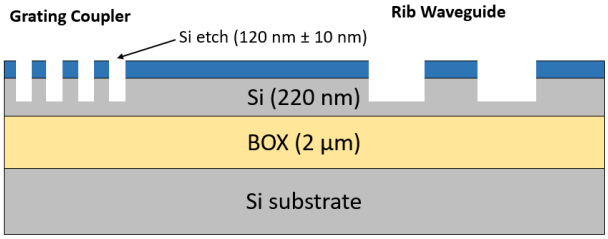
1. Starting SOI substrate



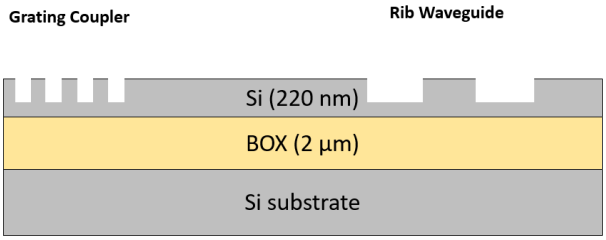

2. Resist patterning for Silicon Etch (GDS layers 3 & 4) – 120 nm ± 10 nm etch



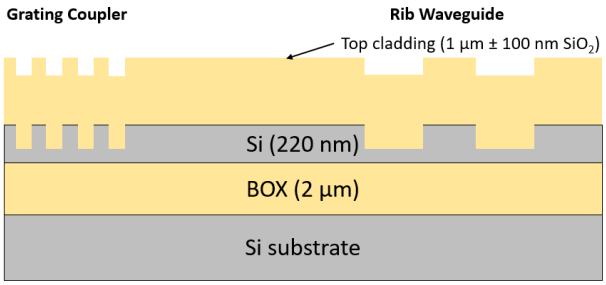

3. Shallow Si etch (120 nm ± 10 nm etch depth)




4. Resist strip



5. Deposition of 1 µm ± 100 nm thick $SiO_2$ top cladding




## 5 DESIGN RULES

It is important that designs conform to the following design rules to ensure clarity and correct processing.

## 5.1 DESIGN AREA

The standard user cell has dimensions of **6 x 3 mm²**, as shown in Figure 1. Each student will receive a single 25 x 33 mm2 chip that contains their designs, in addition to all the designs from other partners in the project, with a schematic of where to find their own design. An illustration is shown below in Figure 1.

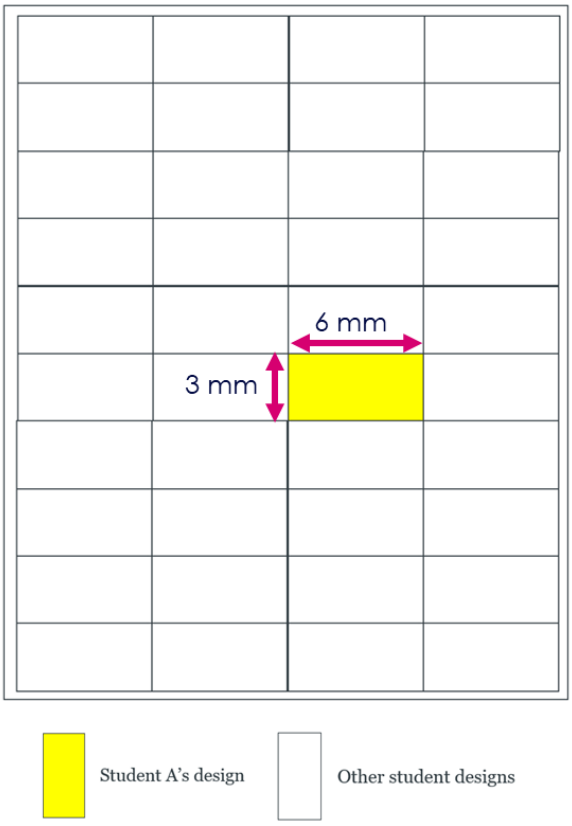



*Figure 1 – An example of a user cell location in the provided chip.*

## 5.2 GDS LAYERS

Each lithographic step in the fabrication process flow is identified by a specific GDS layer/s. These are as follows:

*Silicon Etch – GDS Layer 3 (Light field) & GDS Layer 4 (Dark field) – etch depth: 120 nm ± 10 nm*

This layer defines rib waveguides and grating couplers, and is split into two separate GDS layer numbers, patterned into the same resist and etched together:

*GDS Layer 3*: Drawn objects on this layer will be protected from the silicon etch. Users should draw the waveguides and any other features to remain following 120 nm silicon etching. During fracturing processing, this will be translated into a pattern that defines 5 µm wide trenches on either side of the waveguides drawn in GDS layer 3 (see Figure 2).

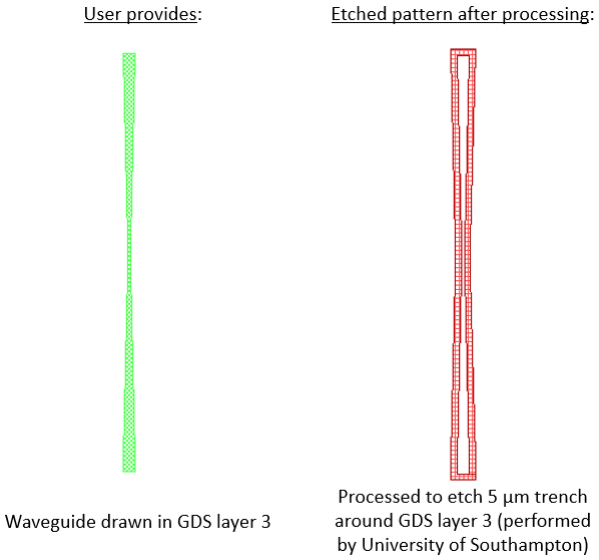



*Figure 2 - Description of GDS Layer 3 processing.*

*GDS Layer 4*: Drawn objects on this layer will be exposed to the 120 nm silicon etch. The layer can be used for structures such as labels and grating couplers.

*Cell Outline – GDS Layer 99*

This layer defines the design space boundaries.

## 5.3 DESIGN RULES SUMMARY

A summary of the design rules and GDS layer numbers described in this section is detailed in Table 1 below.

*Table 1 – Design rules summary.*

| Layer description | GDS number | Field | Minimum feature size | Minimum gap | Max. Feature Width |
|---|---|---|---|---|---|
| Silicon Etch (120 nm ± 10 nm) | 3 | Light | 250 nm | 200 nm | 20 µm |
| | | | 300 nm | 200 nm | N/a |
| | 4 | Dark | 200 nm | 250 nm | 20 µm |
| | | | 200 nm | 300 nm | N/a |
| Cell Outline | 99 | N/a | N/a | N/a | N/a |
| Labels* | 100 | Dark | 250 nm | 250 nm | N/a |

*Features drawn in the Labels layer will be merged into Silicon Etch Layer by the CORNERSTONE team.

A minimum spacing between waveguides of at least 5 µm is recommended to avoid power coupling.

## 5.4 GDSII TEMPLATE FILE

A *.gdsII* template file titled 'Design Template' has been made available containing the information described in this section. Ensure that all submitted designs fit within the specified area, and that only the designated GDS layer numbers are used.

## 5.5 KLAYOUT DESIGN RULE CHECK (DRC)

In order to help you ensure that you comply with the design rules, you can download and execute the KLayout pre-DRC script provided by the University of Southampton Team on our website https://cornerstone.sotonfab.co.uk/mpw/live-calls (note that the automatic DRC will not check all of the design rules, so it remains very important to read the design rules in detail).

It is critical that your submitted mask design does not contain any DRC violations, otherwise it will not be accepted for fabrication and you will have no opportunity to correct it.

## 6 MASK SUBMISSION PROCEDURE

In order to be eligible to submit a design you must first sign-up to this call using the online form found using the link below. This is in order to enable us to prepare the necessary paperwork and plan the fabrication process effectively. The sign-up deadline is found at the top of this document.

https://cornerstone.sotonfab.co.uk/mpw/mpw-sign-up-form/

Under no circumstances will we accept any design submissions for which we have not received a sign-up form.

After completing the sign-up form, when you are ready to submit your mask design on or before the mask submission deadline listed at the top of this document, follow the link below to the CORNERSTONE website mask submission page:

https://cornerstone.sotonfab.co.uk/mpw/gds-file-upload

A purchase order (PO) must be uploaded to this form to pay the access fee.

You must also upload your design file to the submission form. Ensure that the top cell in your design file is titled '*Cell0_[Name]_[Name of Institution]*'.

## 7 MASK PROCESSING PERFORMED BY UNIVERSITY OF SOUTHAMPTON

Upon receipt of your *.gdsII* file, the University of Southampton team will perform the following mask processing steps in order to produce the final mask, based on the descriptions provided in Section 5.1:

*Silicon Etch – GDS Layer 3 (Light field) & GDS Layer 4 (Dark field) – etch depth: 120 nm ± 10 nm*

1. Grow GDS layer 3 by 5 µm in all directions.
2. Subtract GDS layer 3 from the output of (1) to produce the etch trenches around the drawn waveguides.
3. Combine the output of (2) with GDS layer 4 and GDS layer 100.

## 8 TECHNICAL SUPPORT

If you have any questions relating to the fabrication process or design rules, please contact your course instructor or supervisor.