CORNERSTONE DESIGN GUIDELINES
340nm SOI MPW #49 March 2026

SIGN-UP DEADLINE: 15/04/2026
DESIGN SUBMISSION DEADLINE: 13/05/2026
All deadlines end at 13:00 (UK time)

1 TERMS AND CONDITIONS AND COST

All design submissions must agree with the terms and conditions:
www.cornerstone.sotonfab.co.uk/terms-and-conditions
Under no circumstances will we accept designs without agreement with the terms. Therefore, we strongly recommend that the terms and conditions are pre-authorised by your institution prior to the mask submission date.

A purchase order (PO) must be uploaded at the same time as submitting your mask design in order to pay the access fee, detailed in Table 1 below. Purchase orders will not be accepted via email.

Table 1: Access cost and Delivery Time

Design Area [mm^2]	11.47 x 4.9	5.5 x 4.9	Delivery Time
Access Cost with Heaters*	£19,980	£14,700	14 weeks
Access Cost without Heaters*	£12,790	£8,875	14 weeks
Access Cost for UK Enterprises and Academia†	50% off	50% off	14 weeks

Table 2: Additional services

Pick-and-place photodiodes*	Access Cost with Heaters + Service cost	+ 4 weeks

The service cost for photodiodes are detailed in Table 3 for request to have up to 10 PDs per die, on a maximum of 5 dies. The grating couplers underneath PD footprint will remain functional; hence the non-bonded chips will remain operational for fibre-to-chip coupling. Please contact cornerstone@soton.ac.uk for further information.

**Quoted prices are exclusive of VAT, import duties/customs fees, withholding taxes etc.*

University of Southampton
UKRI Engineering and Physical Sciences Research Council
University of Glasgow

Table 3: Cost table for bonded photodiodes

Number of PDs	Service cost per die[#]
1	£750
2-5	£1,500
6-10	£2,500

[#]*The service cost for PD integration is an additional service and falls outside of the terms of the eligible UK Academia/Company discount.*

† Are you from a UK company or academic institution?

UK companies and universities may be eligible for a 50% discount on the cost of this MPW run with support from the CORNERSTONE Photonics Innovation Centre (C-PIC) (EP/Z531066/1), funded by UK Research and Innovation. Support will be provided under the Subsidy Control Act (2022) via Minimal Financial Assistance. To be eligible you will need to demonstrate the potential impact of receiving assistance against one or more of the following categories: impact on jobs and skills, access to technology, accelerating product development. Following submission of your sign-up form, you will receive correspondence with more details of how this support will be provided. For UK companies, the support is only available for first time MPW users with a UK design/development/manufacturing presence and only for prototyping and product development.

To receive Design Rule Check (DRC) feedback from the CORNERSTONE team, users must submit their designs no later than the design submission deadline. **Submissions beyond the design submission deadline will not be included in the MPW run.** The CORNERSTONE team would be grateful for the opportunity to work with you prior to the submission deadline to ensure your designs pass DRC. For more information, please visit our website: www.cornerstone.sotonfab.co.uk/mpw/live-calls/

2 DESIGN RULE CHANGES FROM PREVIOUS CALL (MPW #44)

- Pick-and-place bonded photodiodes are now being offered alongside the standard component library. Layers (140,1), (147/1) and (150/1) presented to help with PD placement.

3 PROCESS DESIGN KIT

CORNERSTONE Process Design Kits (PDK) are available in Luceda Photonics' IPKISS software, GDSFactory, Cadence Virtuoso and L-Edit. PDKs for all CORNERSTONE technology platforms are freely accessible via Wave Photonics' portal. To obtain free access to the PDKs in your preferred software tool, please visit www.wavephotonics.com.

Wave Photonics also provides Scattering Parameters to enable full circuit simulation. For more information, please contact Wave Photonics support at info@wavephotonics.com.

To obtain a copy of the software and a license key for IPKISS, please contact Luceda by sending an email to info@lucedaphotonics.com, specifying that you require a license for CORNERSTONE PDK usage. Luceda will contact you within 1-2 working days following the receipt of your request to provide a quote for the license. Of course, if you already have a valid license, the PDK can be accessed free of charge. The IPKISS platform enables the automation and integration of all aspects of your photonic design flow in one tool, using one standard language. The PDK can be used in either IPKISS' Python coding environment or in the GUI of Siemens EDA L-Edit by using the IPKISS Link for Siemens EDA. For more information, please visit www.lucedaphotonics.com.

A library of building blocks is also available for download in .gdsII format on the CORNERSTONE website at https://cornerstone.sotonfab.co.uk/mpw/live-calls/.

4 PROCESS FLOW

For this call, the patterns will be processed on a single-side polished Silicon-on-Insulator (SOI) wafer, with the following nominal parameters:

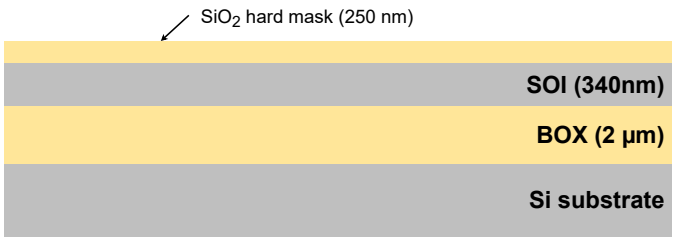
- Crystalline silicon (Si) substrate with resistivity of 750 Ω.cm
- Thermal silica (SiO_2) **B**uried **OX**ide (BOX) layer with a thickness h_{BOX} = 2 µm
- Crystalline Silicon (Si) core layer (100)-oriented with a thickness h_{wg}= 340 ± 20nm

We will offer two silicon etch process: 1) a shallow silicon etch of 140 ± 10 nm, and 2) a full silicon etch to the BOX layer. We will offer a 1 µm±100 nm-thick silicon dioxide top cladding layer with two metal layers for heaters: 1) titanium nitride (TiN) heater filaments, and 2) titanium/aluminium (Ti/Al) heater contact pads. Finally, we will offer

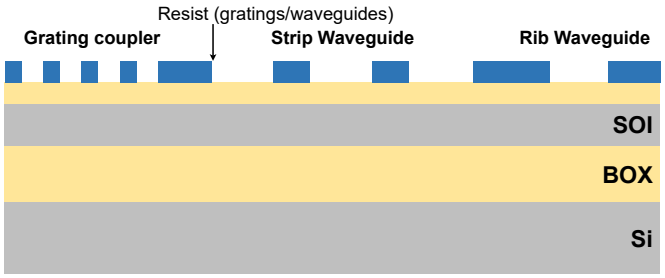
The schematic description of the process flow is given below:

1. Starting SOI substrate

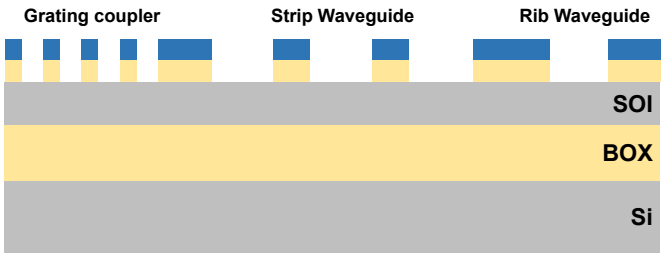
2. Silicon dioxide hard mask deposition - 250 nm



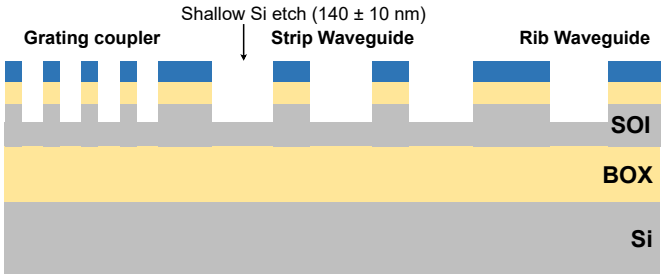
3. Resist patterning for SOI Etch 1 (GDS layer 3,4 & 6) – 140 ± 10 nm etch



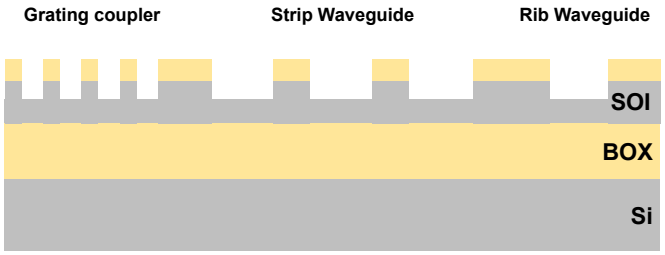
4. Hard mask etch



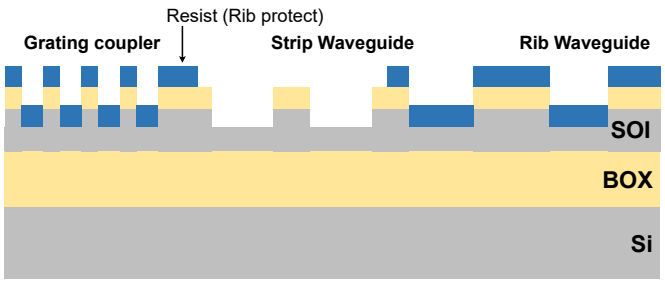
5. Shallow Si etch (140 ± 10 nm etch depth)



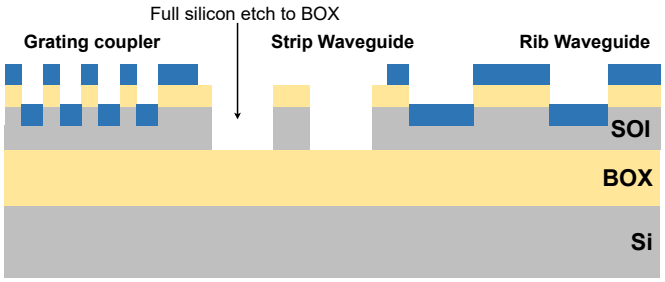
6. Resist strip



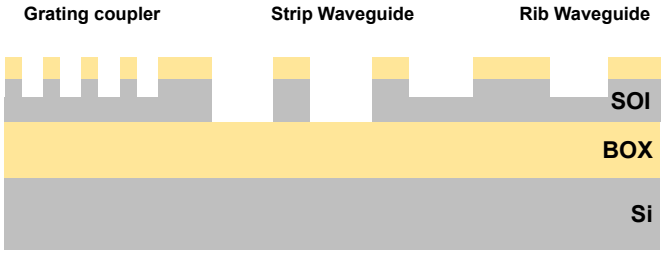
7. Resist patterning for SOI Etch 2 (GDS layer 5) – 200 nm etch to BOX



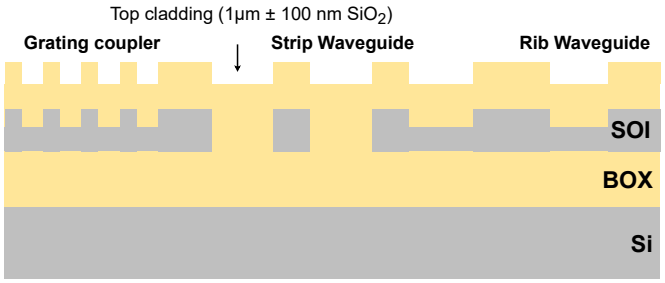
8. Rib-to-strip Si etch (200 nm to BOX)



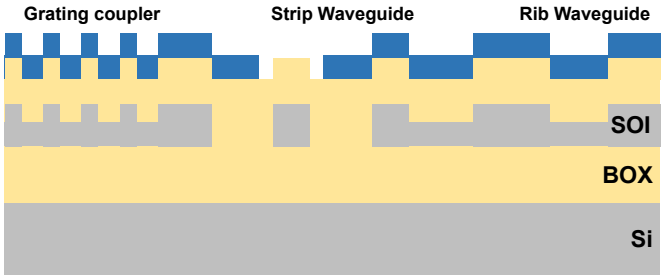
9. Resist strip



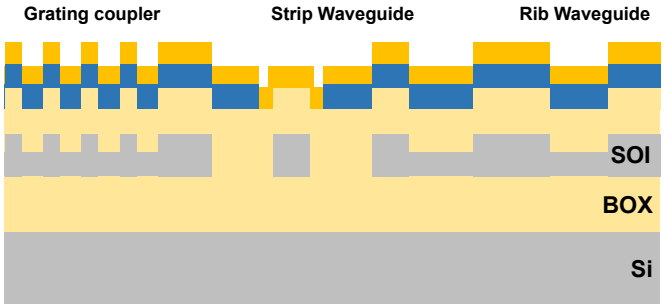
10. Deposition of 1 µm±100 nm-thick SiO_2 top cladding



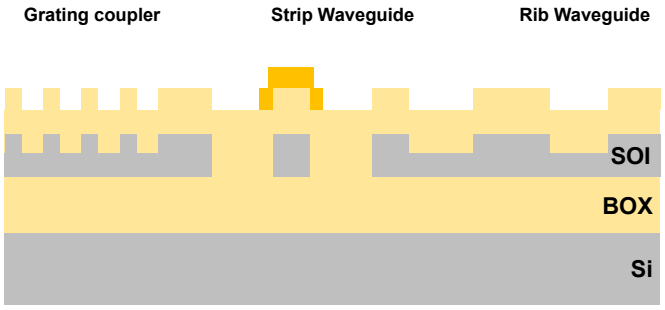
11. Resist patterning for Heater Filaments (GDS layer 39)



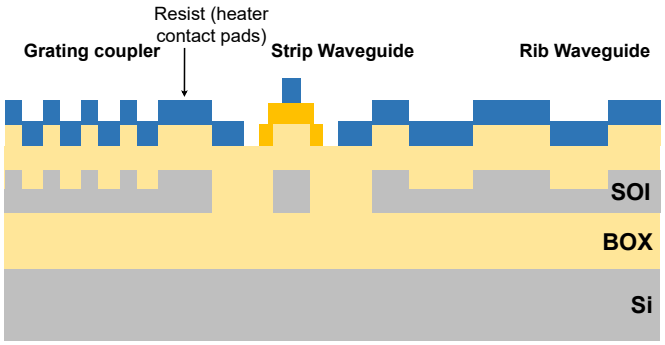
12. Heater filament deposition



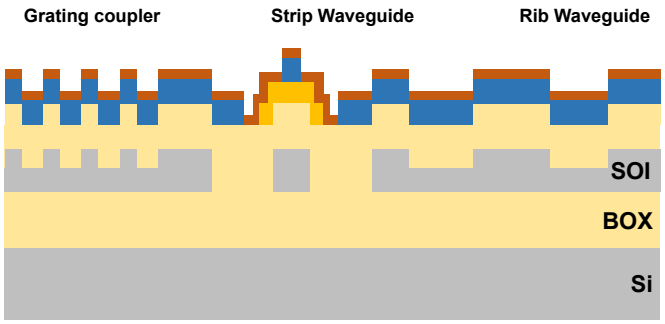
13. Metal lift-off



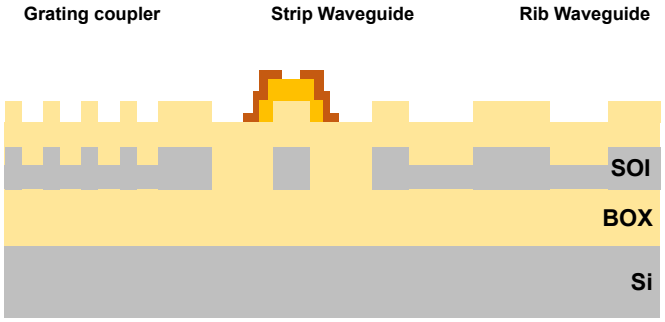
14. Resist patterning for Heater Contact Pads (GDS layer 41)



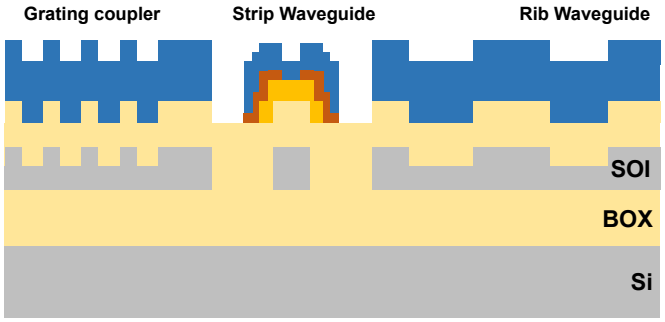
15. Heater contact pads deposition



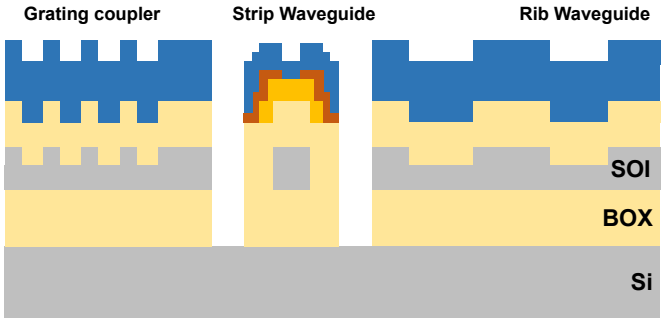
16. Metal lift-off



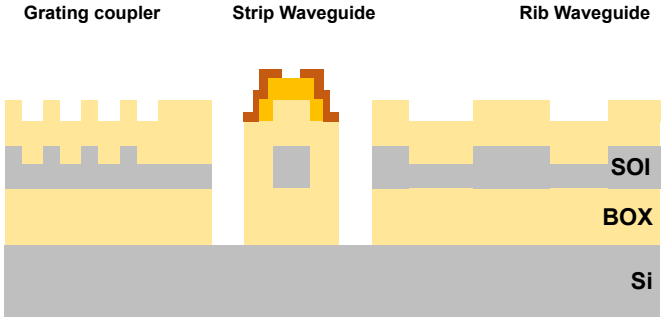
17. Resist patterning for heater isolation trench (GDS layer 46)



18. Silicon dioxide etch to the silicon substrate



19. Resist strip

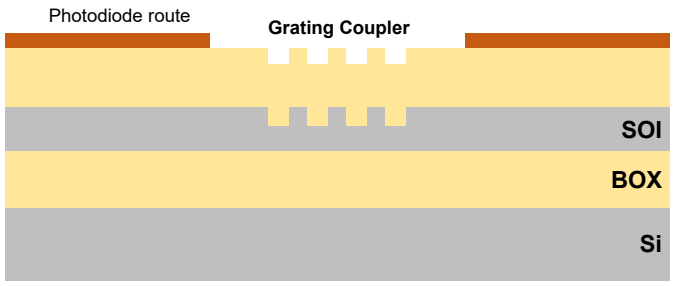


If you require any alternative processing steps (e.g. custom etch depths), we may be able to perform them for a suitable charge. Email cornerstone@soton.ac.uk with your request.

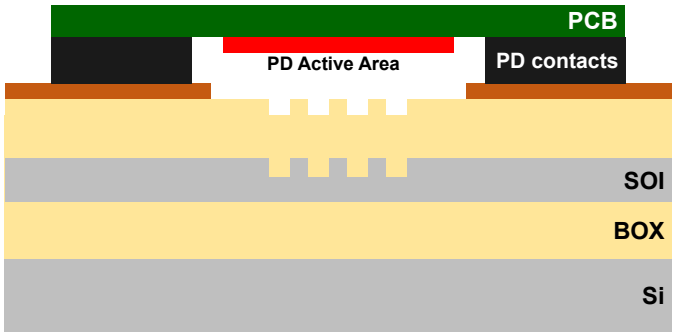
4.1 PHOTODIODE INTEGRATION

The photodiode integration will be done in the facilities of University of Glasgow using a pick-and-place flow. Owing to the double-sided detection capabilities of the photodiodes used, it is possible to route the electrical outputs before the photodiode bonding (without a post-bond redistribution layer). As the routing will necessitate metallisation during wafer-scale fabrication, opting in for PD integration will directly imply an access cost with heaters involved. The related process flow is described below.

1. Starting with the patterned SOI (220nm) with cladding (1 µm±100nm), with routing on Layer 41:



2. The PD is bonded directly to the routing on Layer 41.



5 DESIGN RULES

It is important that designs conform to the following design rules to ensure clarity and correct processing.

5.1 DESIGN AREA

The standard user cell has dimensions of **11.47 x 4.9 mm^2** or **5.5 x 4.9 mm^2**.

5.1.1 PHYSICAL DIE SIZE

The physical size of the dies you will receive is approximately 12.5 x 5.3-5.6 mm^2. This area includes a border the CORNERSTONE team will add that contains alignment marks, metrology boxes etc. which surround 3x design areas from various CORNERSTONE users, as shown in Figure 1. If you require specific physical die dimensions (12.5 x 5.3 mm^2 or 12.5 x 5.6 mm^2), for example if integration to a PCB is required, please specify the physical die dimensions you require in the online mask submission form you are required to complete as part of the submission process (see Section 8).

5.2 GDS LAYERS

Each lithographic step in the fabrication process flow is identified by a specific GDS layer/s. These are as follows:

Process layers: Patterns on these layers will be transferred (directly or indirectly) onto the chips during fabrication.

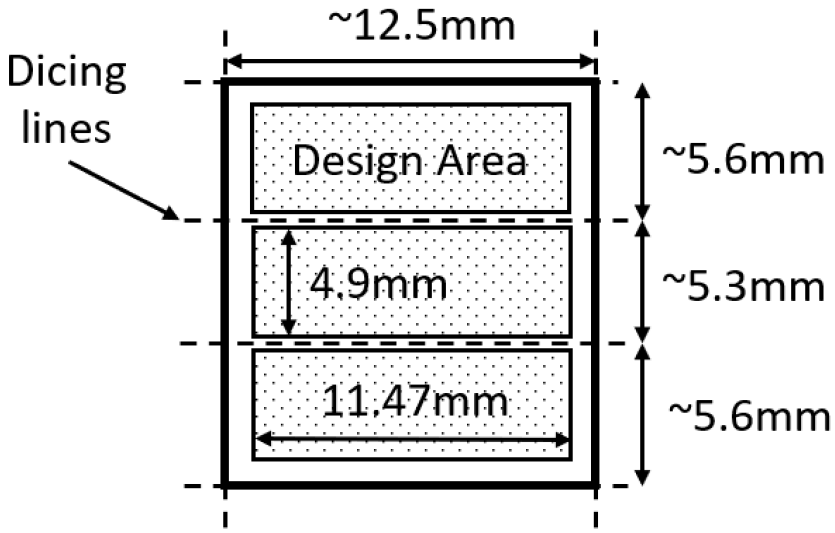


Figure 1: Physical die dimensions.

Silicon Etch 1 (Grating & Waveguide layer) - etch depth: 140 ± 10 nm

This layer is used to define grating couplers as well as both strip and rib waveguides (to form a rib waveguide, the slab region is protected during Silicon Etch 2, defined by GDS layer 5 – see below), and is split into three separate GDS layer numbers, patterned into the same resist and etched together:

GDS Layer 3 (Waveguide light-field):

Drawn objects on this layer will be protected from the silicon etch. Users should draw the waveguides and any other features to remain following 120 nm silicon etching (to the rib waveguide height). During fracturing processing, this will be translated into a pattern that defines 5 µm-wide trenches on either side of the waveguides drawn in GDS Layer 3 (see Figure 2).

If you require waveguide trenches that are a different width, refer to the guidelines for generating the trenches in Section 9. You can complete these steps yourself and modify the growth function dimension in step 1.

GDS Layer 4 (Waveguide dark-field):

Drawn objects on this layer will be exposed to the 120 nm silicon etch (to the rib waveguide height). An example photonic crystal structure is shown in Figure 3. The important thing to note here is that the waveguide layer drawn in GDS Layer 3 should overlap the structures drawn in GDS Layer 4, so that when the 5 µm-wide trenches are generated by CORNERSTONE, a continuous waveguide remains.

GDS Layer 6 (Grating dark-field):

Drawn objects on this layer will be exposed to silicon etch to define grating couplers, which are fabricated with 140 nm shallow silicon etching. The drawn area is etched.

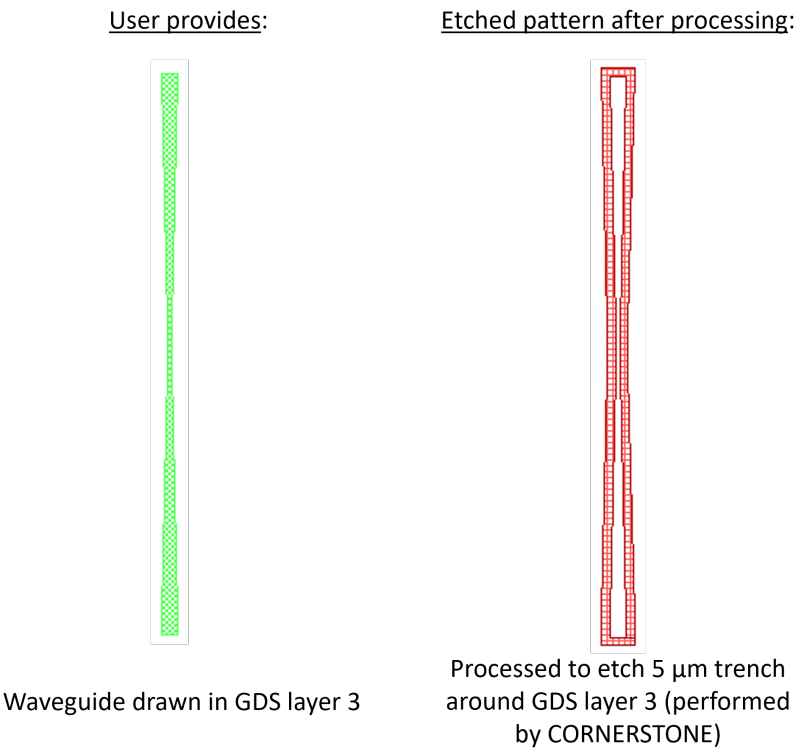


Figure 2: Description of GDS Layer 3 processing.

Silicon Etch 2 (Rib protect layer) – GDS Layer 5 (light-field) – etch depth: 200 nm to BOX:

This layer defines the protective layer for rib waveguides. Drawn objects in this layer will be protected from etching whilst the strip waveguides are etched to the BOX (all areas not previously defined in the Silicon Etch 1 Layer will be protected from etching by a hard mask). We recommend that this layer should extend more than or equal to 5 µm from the edge of features drawn in GDS Layer 3 so that the 5 µm-wide trenches etched in the previous partial silicon etching step are fully protected by GDS layer 5, with the exception of any rib-to-strip transitions. An overview of how to draw both strip and rib waveguides is shown in Figure 4.
All grating couplers (GDS layer 6) should also be protected with GDS layer 5.

Heater Filaments – GDS Layer 39 (light-field): This layer defines the heater filaments. Drawn objects on this layer will remain after metal lift-off. It is recommended to use a filament width of 900 nm for the best compromise between heater power efficiency, phase tunability and robustness.

Heater Contact Pads – GDS Layer 41 (light-field): This layer defines the heater contact pads. Drawn objects on this layer will remain after metal lift-off. An example heater layout for a straight waveguide is included in the *.gdsII* template file. The contact pads can be modified according to your probe design.

Isolation Trenches – GDS Layer 46 (dark-field): This layer defines deep etched isolation trenches around the heater filaments (GDS layer 39). Drawn objects in this layer will

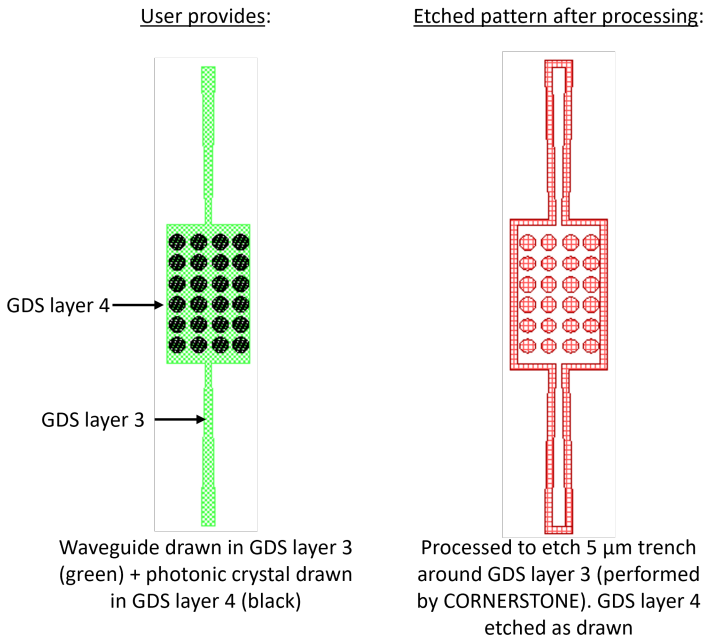


Figure 3: Example photonic crystal structure using GDS Layers 3 & 4.

be exposed to silicon dioxide etching to the Si substrate.

Labels – GDS Layer 100: This layer defines text labels, which will be merged with Silicon Etch 2 layer by the CORNERSTONE team. This layer will not have any design rule checking (DRC) performed.

Information layers: These layers are purely informative and their contents will not be transferred onto the chips during fabrication.

Physical PD Area – GDS Layer 140/1: This layer shows the physical boundary of the bonded PD on the finalised chips.

PD Active Area – GDS Layer 147/1: This layer shows the active area of the photodiodes for the convenience of the user.

PD Exclusion Zone - GDS Layer 150/1: This layer shows the exclusion zone for a single PD. Packaging DRC checks will solely include this layer.

Cell Outline – GDS Layer 99: This layer defines the design space boundaries (11.47 x 4.9 mm^2 or 5.5 x 4.9 mm^2).

Note: You do not need to add fabrication alignment marks to your design. Layer-to-layer alignment marks will be added by the CORNERSTONE team, placed outside the design area.

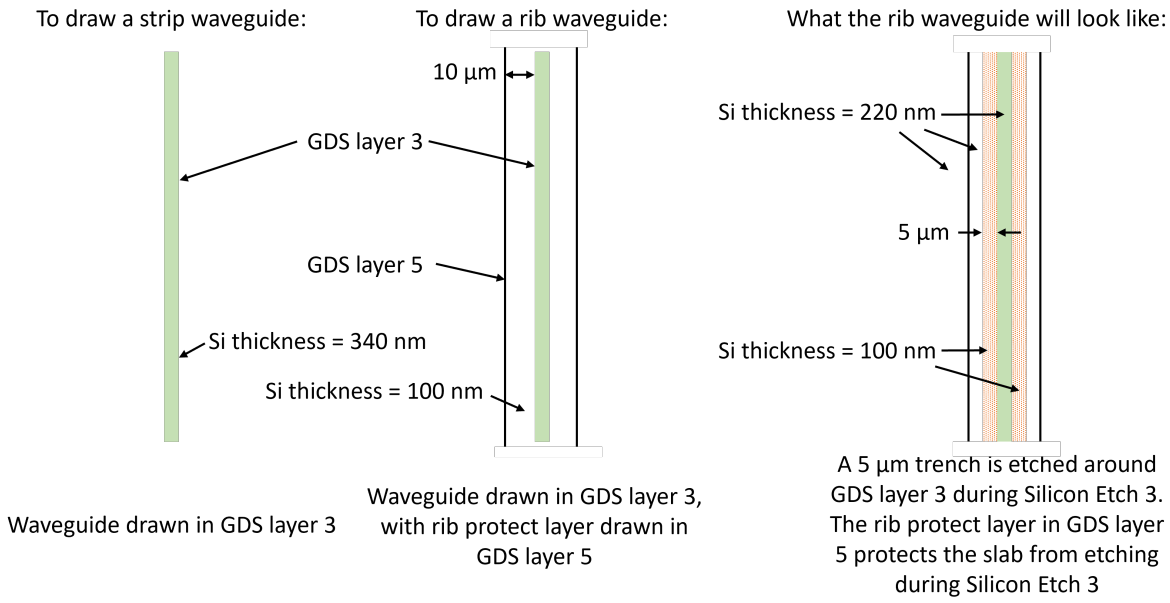


Figure 4: Drawing strip and rib waveguides.

5.3 MINIMUM FEATURE SIZES AND OTHER DESIGN RULES

- Minimum feature sizes, minimum gaps, and maximum feature widths for each GDS layer are detailed in Table 4.
- A minimum spacing between waveguides of at least 5 µm is recommended to avoid power coupling.
- All structures drawn in GDS Layer 6 must overlap by at least 200 nm with GDS Layer 3 (Waveguides).
- All structures drawn in GDS layer 6 (if they are grating couplers) must overlap by at least 200 nm with GDS layer 3 (Waveguides) to account for alignment errors, and with GDS layer 5 (rib protect layer) to prevent the grating couplers becoming fully etched during Silicon Etch 2.
- An overlap of at least 10 µm between GDS layer 39 (Heater Filaments) and GDS layer 41 (Heater Contact Pads) is recommended for optimal heater performance.
- Ensure all structures drawn in GDS layer 6 (Grating Couplers) do not overlap with either GDS layer 39 (Heater Filaments) or GDS 41 (Heater Contact Pads).
- GDS layer 46 should not overlap with Waveguides (GDS layer 3) & there should be a minimum distance of 200 nm between GDS layer 46 and GDS layer 3.
- GDS layer 46 should not overlap with Heater Filaments (GDS layer 39) & there should be a minimum distance of 200 nm between GDS layer 46 and GDS layer 39.
- GDS layer 46 should not overlap with Heater Contact Pads (GDS layer 41) & there should be a minimum distance of 200 nm between GDS layer 46 and GDS layer 41.

- The PD-related layers of GDS 140/1,147/1 & 150/1 will not be checked with DRC explicitly.

5.4 DESIGN RULES SUMMARY

A summary of the design rules and GDS layer numbers described in this section is detailed below.

Table 4: Access cost and Delivery Time

Layer Description	GDS Number	Field	Min. Feature Size	Min. Gap	Max. Feature Length
Silicon Etch 1	3/0	Light	350 nm	200 nm	N/A
	4/0	Dark	200 nm	350 nm	
	6/0*	Dark	200 nm	250 nm	20 µm
			200 nm	350 nm	N/A
Silicon Etch 2 (200 nm to BOX)	5/0	Light	350 nm	200 nm	N/A
Heater Filaments	39/0	Light	600 nm	10 µm	N/A
Heater Contact Pads	41/0	Light	2 µm	10 µm	N/A
Isolation trench	46/0	Dark	5 µm	2 µm	N/A
Physical PD Area	140/1	N/A	N/A	N/A	N/A
PD Active Area	147/1	N/A	N/A	N/A	N/A
PD Exclusion Zone	150/1	N/A	N/A	N/A	N/A
Cell Outline	99/0	N/A	N/A	N/A	N/A
Labels†	100/0	Dark	250 nm	250 nm	N/A

**For the grating layer there is a maximum feature length restriction of 20 µm when the minimum gap is 250 nm. This is because resist features that are long and thin can collapse during the development process. Resist gaps of $>$ 350 nm are stable and therefore there are no length restrictions for widths $>$ 350 nm.*

†Features drawn in the Labels layer will be merged into the Silicon Etch 2 layer by the CORNERSTONE team.

In order to help you ensure that you comply with the design rules, you can download and execute the KLayout pre-DRC script provided by CORNERSTONE on our website www.cornerstone.sotonfab.co.uk/mpw/live-calls/ (note that the automatic DRC will not check all of the design rules, so it remains very important to read the design rules in detail.)
MPW users will have an opportunity to attend 1-to-1 Drop-in Session to pre-review mask layouts before the submission deadline, using the link to book a 20-min session.

5.5 FILE FORMAT

Designs must be submitted in a Graphical Database System file (extension *.gdsII*) or Open Artwork System Interchange Standard (extension *.oas*) format. Ensure a manufacturing grid size of 1 nm is used, as per the CORNERSTONE GDSII Template file.

We recommend dedicated lithography editing software be used in the design of the *.gdsII* or *.oas* file.

5.6 GDSII TEMPLATE FILE

A *.gdsII* template file has been made available on our website containing the information described in this section. Ensure that all submitted designs fit within the specified area, and that only the designated GDS layer numbers are used.

6 MATERIAL PROPERTIES

The measured refractive indices of Silicon and SiO_2 layers are as shown in Figure 5 below. This data is also available in tabular format on our website.

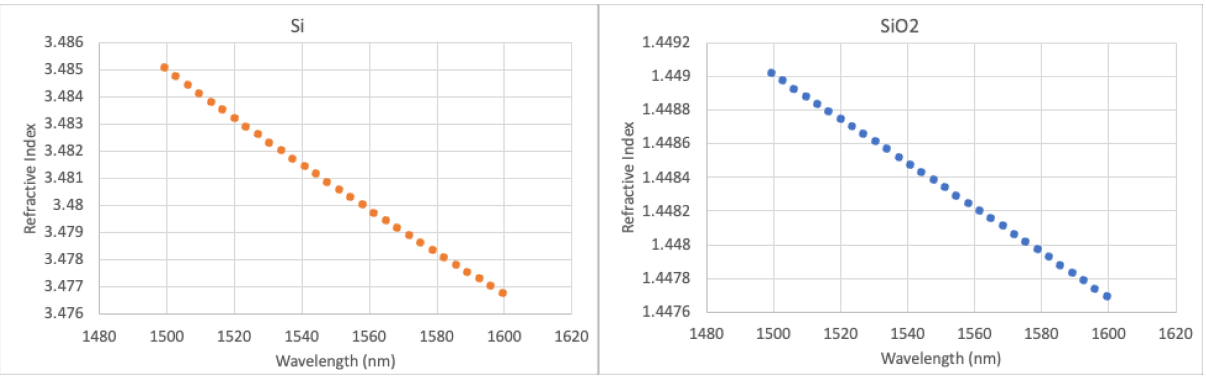


Figure 5: Refractive indices of Silicon (left) and SiO_2 (right)

7 QUALITY ASSESSMENT

This fabrication run will be qualified by characterising a standard test pattern that is included on the chip (not part of the user cell). The test structures that will be checked after fabrication are reported in Table 5, together with the values that are targeted by the CORNERSTONE platform.

Table 5: Quality assessment parameters

Test Structure	Parameter	Value
Straight single mode strip waveguide	Propagation loss	$<$ 5 dB/cm for TE mode in C-band
Straight single mode rib waveguide	Propagation loss	$<$ 3 dB/cm for TE mode in C-band
MZI integrated with the PDK heater	Phase shift efficiency	$<$ 30 mW/π phase shift
MZI integrated with the PDK heater with isolation trench	Phase shift efficiency	$<$ 15 mW/π phase shift
Integrated photodiode	Responsivity	$>$ 0.5 A/W @ λ =1550 nm

8 MASK SUBMISSION PROCEDURE

In order to be eligible to submit a design you must first sign-up to this call using the online form found using the link below. This is in order to enable us to prepare the necessary paperwork and plan the fabrication process effectively. The sign-up deadline is found at the top of this document.

www.cornerstone.sotonfab.co.uk/home/mpw-sign-up-form

Under no circumstances will we accept any design submissions for which we have not received a sign-up form.

After completing the sign-up form, when you are ready to submit your mask design on or before the mask submission deadline listed at the top of this document, follow the link below to the CORNERSTONE website mask submission page:

www.cornerstone.sotonfab.co.uk/gds-file-upload

A purchase order (PO) must be uploaded to this form to pay the access fee. Purchase orders will not be accepted via email.

You must also upload your design file to the submission form. Ensure that the top cell in your design file is titled '*Cell0_[Name of Institution]*'.

For information about setting up CORNERSTONE as a supplier to your institution, or if you encounter any problems with the online forms, please contact cornerstone@soton.ac.uk

9 MASK PROCESSING PERFORMED BY CORNERSTONE

Upon receipt of your *.gdsII* file, the CORNERSTONE team will perform the following mask processing steps in order to produce the final mask, based on the descriptions provided in Section 5.2.

Silicon Etch 1 GDS 3-4 (Waveguide, light/dark-field) & GDS 6 (Grating, dark-field):

1. Grow Waveguide layer (GDS Layer 3) by 5 µm in all directions.
2. Subtract the Waveguide layer (GDS Layer 3) from the output of (1) to produce the etch trenches around the drawn waveguides.
3. Merge the output of (2) with the dark-field Waveguide layer (GDS Layer 4), dark-field Grating layer (GDS Layer 6), dark-field Heater Isolation Trench layer (GDS Layer 46) and the Labels layer (GDS Layer 100).

Silicon Etch 2 (Rib Protect layer) GDS Layer 5 (light-field) - etch depth: 200nm to BOX:

1. Create a temporary layer by growing the Grating layer (GDS Layer 6) by 200 nm in all direction.
2. Merge the output of (1) with the Rib Protect layer (GDS Layer 5).
3. Subtract the output of (2) from the Cell Outline (GDS Layer 99) to convert to a dark-field mask.
4. Subtract the Heater Isolation Trench layer (GDS Layer 46) from the output of (3).

10 TECHNICAL SUPPORT

If you have any questions relating to the fabrication process or design rules, please contact the CORNERSTONE team (cornerstone@soton.ac.uk).

11 DEVICE DELIVERY

A total of 10 replica cells will be delivered to each user. The delivery time schedule can be found in Table 1.

12 FEEDBACK

Feedback is essential to the CORNERSTONE team. It is required to ensure a continuous improvement to the quality of our services. It is also evidence on the user satisfaction, and a measure to what extent we were able to meet user requirements. Therefore, we kindly ask our users to provide feedback to us, including device performance data, SEM images, future interests for the CORNERSTONE project etc. A feedback form will be sent to you along with your chips.

Alternatively, email cornerstone@soton.ac.uk with your comments.

13 PUBLICATIONS

If you are benefitting from subsidised access via the C-PIC funding, please include the following statement in the "Funding" section of any publications:

> "The chip fabrication for this research was funded by the Engineering and Physical Sciences Research Council (EPSRC) C-PIC (EP/Z531066/1) project."

This is important to us to be able to demonstrate impact from the funding. If you are a paying user, we kindly ask that you include CORNERSTONE in the **"Acknowledgments"** section of any publications that result from the chips you receive from CORNERSTONE.