

CORNERSTONE DESIGN GUIDELINES

Silicon Nitride 300nm MPW #13 June 2026



SIGN-UP DEADLINE: 15/07/2026

DESIGN SUBMISSION DEADLINE: 12/08/2026

All deadlines end at 13:00 (UK time)

1 TERMS AND CONDITIONS AND COST

All design submissions must agree with the terms and conditions:

www.cornerstone.sotonfab.co.uk/terms-and-conditions

Under no circumstances will we accept designs without agreement with the terms. Therefore, we strongly recommend that the terms and conditions are pre-authorized by your institution prior to the mask submission date.

A purchase order (PO) must be uploaded at the same time as submitting your mask design in order to pay the access fee and any additional services, detailed in Tables 1 & 2. Purchase orders will not be accepted via email.

Table 1: Access cost and Delivery Time

Design Area [mm ²]	11.47 x 15.45	Delivery Time
Access Cost with Heaters*	£19,980	12 weeks
Access Cost without Heaters*	£9,470	12 weeks
Access Cost for UK Enterprises and Academia†	50% off	12 weeks

Table 2: Additional services

Flip-chip bonded photodiodes*	Access Cost with Heaters + Service cost	+ 4 weeks
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The service cost for photodiodes are detailed in Table 3 for request to have up to 10 PDs per die, on a maximum of 5 dies. The grating couplers underneath PD footprint will remain functional; hence the non-bonded chips will remain operational for fibre-to-chip coupling. Please contact cornerstone@soton.ac.uk for further information.

*Quoted prices are exclusive of VAT, import duties/customs fees, withholding taxes etc.

Table 3: Cost table for flip-chip bonded photodiodes

Number of PDs	Service cost per die [#]
1	£750
2-5	£1,500
6-10	£2,500

[#]The service cost for PD integration is an additional service and falls outside of the terms of the eligible UK Academia/Company discount.

† **Are you from a UK company or academic institution?**

UK companies and universities may be eligible for a 50% discount on the cost of this MPW run with support from the CORNERSTONE Photonics Innovation Centre (C-PIC) (EP/Z531066/1), funded by UK Research and Innovation. Support will be provided under the Subsidy Control Act (2022) via Minimal Financial Assistance. To be eligible you will need to demonstrate the potential impact of receiving assistance against one or more of the following categories: impact on jobs and skills, access to technology, accelerating product development. Following submission of your sign-up form, you will receive correspondence with more details of how this support will be provided. For UK companies, the support is only available for first time MPW users with a UK design/development/manufacturing presence and only for prototyping and product development. To receive Design Rule Check (DRC) feedback from the CORNERSTONE team, users must submit their designs no later than the design submission deadline. Submissions received after the design submission deadline will not be checked against design rules; therefore, any fabrication failures related to design rule violations will be at the users' own risk. The CORNERSTONE team would be grateful for the opportunity to work with you prior to the submission deadline to ensure your designs pass DRC. For information about setting up CORNERSTONE as a supplier to your institution, please contact cornerstone@soton.ac.uk

2 DESIGN RULE CHANGES FROM PREVIOUS CALL (MPW #12)

- A warning rule is added to the DRC script for dense waveguide regions overlaying cladding opening sections.
- Minimum gap limit for filaments (GDS 39/0) and contact pads (GDS 41/0) were reduced to 5 µm from 10 µm.

3 PROCESS DESIGN KIT

CORNERSTONE Process Design Kits (PDK) are available in Luceda Photonics' IPKISS software, GDSFactory, Cadence Virtuoso and L-Edit. PDKs for all CORNERSTONE technology platforms are freely accessible via Wave Photonics' portal. To obtain free access

to the PDKs in your preferred software tool, please visit www.wavephotonics.com.

Wave Photonics also provides Scattering Parameters to enable full circuit simulation. For more information, please contact Wave Photonics support at info@wavephotonics.com.

To obtain a copy of the software and a license key for IPKISS, please contact Luceda by sending an email to info@lucedaphotonics.com, specifying that you require a license for CORNERSTONE PDK usage. Luceda will contact you within 1-2 working days following the receipt of your request to provide a quote for the license. Of course, if you already have a valid license, the PDK can be accessed free of charge. The IPKISS platform enables the automation and integration of all aspects of your photonic design flow in one tool, using one standard language. The PDK can be used in either IPKISS' Python coding environment or in the GUI of Siemens EDA L-Edit by using the IPKISS Link for Siemens EDA. For more information, please visit www.lucedaphotonics.com.

A library of building blocks is also available for download in .gdsII format on the CORNERSTONE website:

<https://cornerstone.sotonfab.co.uk/mpw/live-calls/>.

4 PROCESS FLOW

For this call, the patterns will be processed on a single-side polished SiN-on-Insulator (SiNOI) wafer, with the following nominal parameters:

- Crystalline silicon (Si) substrate
- Thermal silica (SiO₂) Buried OXide (BOX) layer with a thickness $h_{\text{BOX}} = 3 \mu\text{m}$
- LPCVD Silicon Nitride (SiN) core layer $h_{\text{wg}} = 300 \pm 15 \text{ nm}$

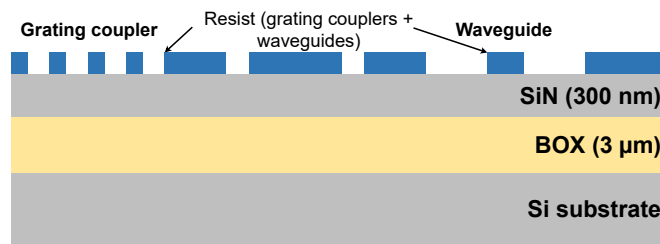
We will offer one silicon nitride etch process: 1) a full silicon nitride etch to the BOX layer. We will offer a $2 \mu\text{m} \pm 200 \text{ nm}$ -thick silicon dioxide top cladding layer with two metal layers for heaters: 1) heater filaments, and 2) heater contact pads. Finally, we will offer a top cladding opening performed by a silicon dioxide etch.

The schematic description of the process flow is given below:

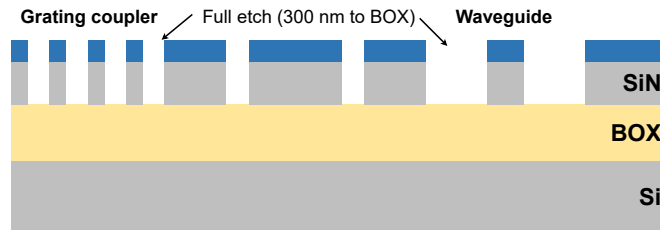
1. Starting SiNOI substrate



2. Resist patterning for SiN Etch (GDS layers 203 & 204) – 300 nm etch to BOX



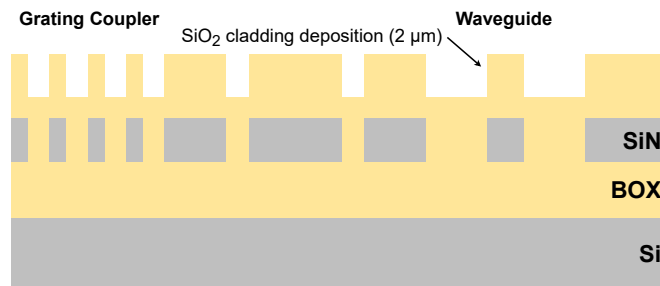
3. SiN Etch (300 nm etch to BOX)



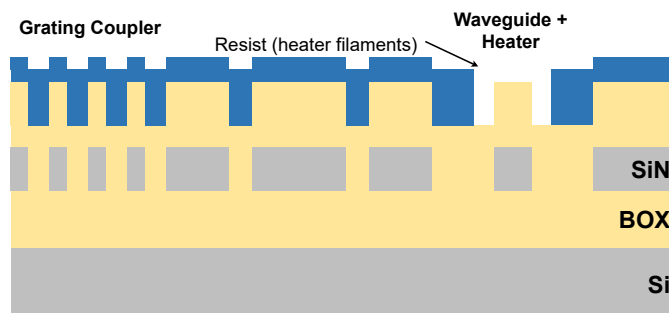
4. Resist strip



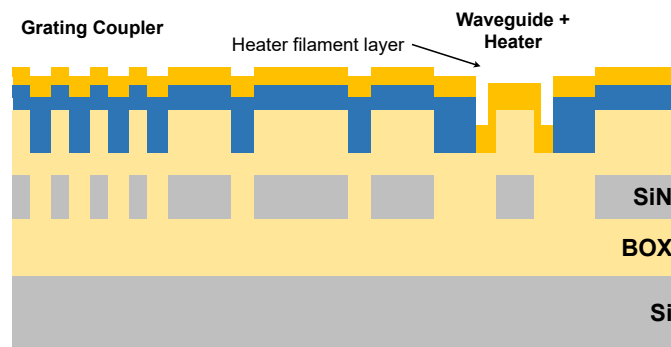
5. Silicon dioxide cladding deposition (2 μm)



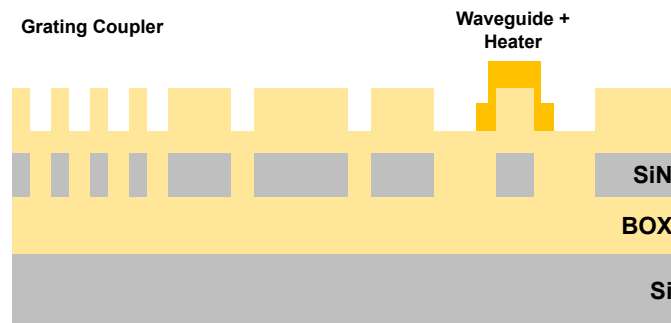
6. Resist patterning for Heater Filaments (GDS layer 39)



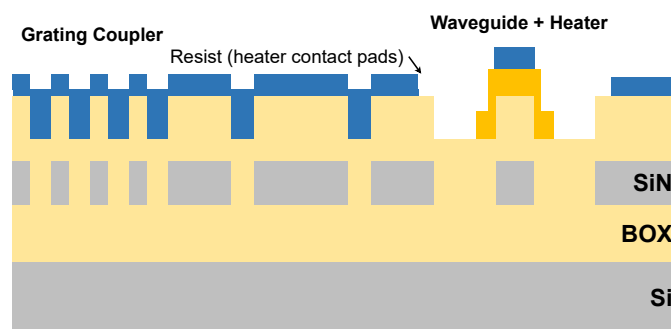
7. Heater filament deposition



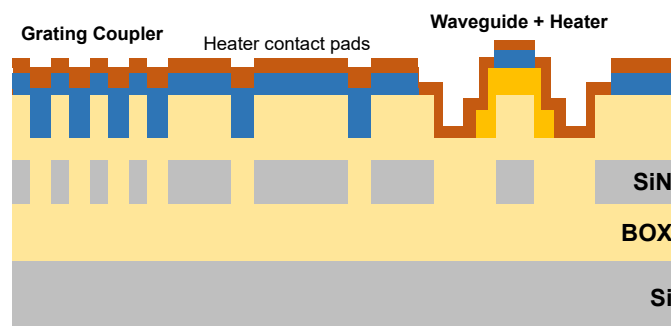
8. Metal lift-off



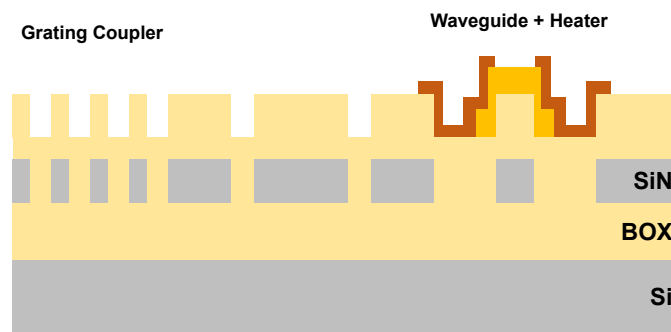
9. Resist patterning for Heater Contact Pads (GDS layer 41)



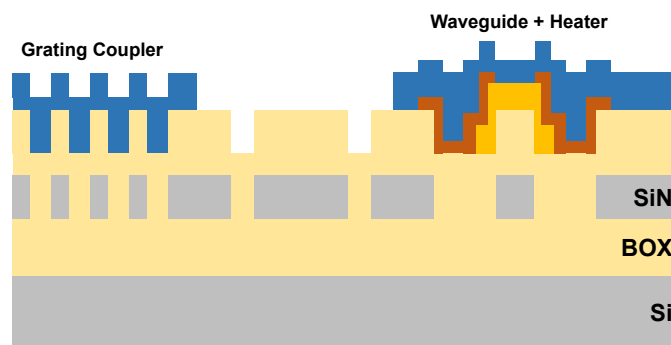
10. Heater contact pads deposition



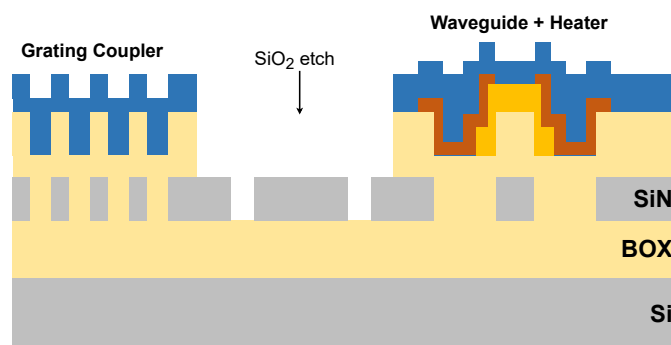
11. Metal lift-off



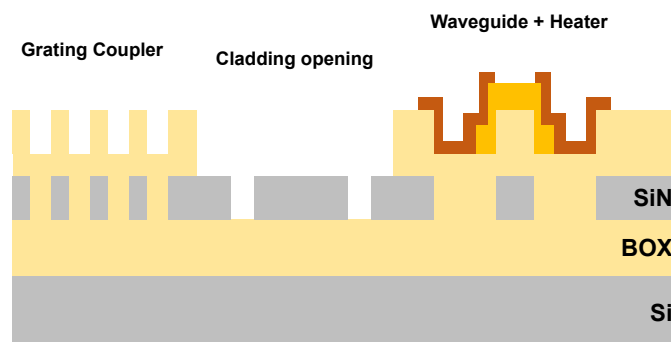
12. Resist patterning for cladding opening window (GDS layer 22)



13. Silicon dioxide etch (2 μm)



14. Resist strip

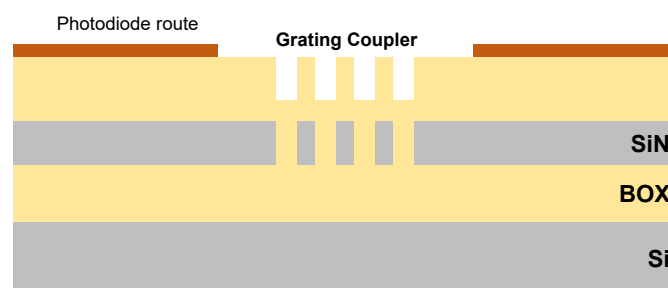


If you require any alternative processing steps (e.g. custom etch depths), we may be able to perform them for a suitable charge. Email cornerstone@soton.ac.uk with your request.

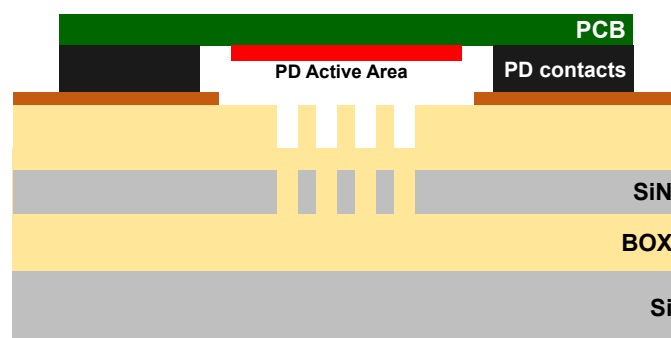
4.1 PHOTODIODE INTEGRATION

The photodiode integration will be done in the facilities of University of Glasgow using flip-chip bonding. Owing to the double-sided detection capabilities of the photodiodes used, it is possible to route the electrical outputs before the photodiode bonding (without a post-bond redistribution layer). As the routing will necessitate metallisation during wafer-scale fabrication, opting in for PD integration will directly imply a access cost with heaters involved. The related process flow is described below.

1. Starting with the patterned SiNOI (300nm) with cladding ($2\ \mu\text{m}\pm 200\text{nm}$), with routing on Layer 41:



2. The PD is bonded directly to the routing on Layer 41.



5 DESIGN RULES

It is important that designs conform to the following design rules to ensure clarity and correct processing.

5.1 DESIGN AREA

The standard user cell has dimensions of **11.47 x 15.45 mm²**.

5.1.1 PHYSICAL DIE SIZE

The physical size of the dies you will receive is approximately 12.5 x 16.5 mm². This area includes a border the CORNERSTONE team will add that contains alignment marks,

metrology boxes etc. If you require specific physical die dimensions, for example if integration to a PCB is required, please specify the physical die dimensions you require in the online mask submission form you are required to complete as part of the submission process (see Section 8).

5.2 GDS LAYERS

Each lithographic step in the fabrication process flow is identified by a specific GDS layer/s. These are as follows:

Process layers: Patterns on these layers will be transferred (directly or indirectly) onto the chips during fabrication.

Silicon Nitride Etch 1: 300 nm full etch to BOX:

This etch is defined for implementing both the strip waveguides as well as the grating couplers. For user convenience, the process layers are split into two separate GDS layer numbers, patterned into the same resist and etched together:

GDS Layer 203 (Light field):

Drawn objects on this layer will be protected from the silicon nitride etch. Users should draw the waveguides and any other features to remain following the full silicon nitride etching. During fracturing processing, this will be translated into a pattern that defines 5 μm -wide trenches on either side of the waveguides drawn in GDS layer 203 (see Figure 1).

If you require waveguide trenches that are a different width, refer to the guidelines for generating the trenches in Section 9. You can complete these steps yourself and modify the growth function dimension in step 1.

GDS Layer 204 (Dark field):

Drawn objects on this layer will be exposed to the full SiN etch to BOX. An example photonic crystal structure is shown in Figure 2. The important thing to note here is that the waveguide layer drawn in GDS Layer 203 should overlap the structures drawn in GDS Layer 204, so that when the 5 μm -wide trenches are generated by CORNERSTONE, a continuous waveguide remains. Note that the client should contact CORNERSTONE team if the design has photonic crystals structures with a diameter smaller than 600 nm to decide on whether structures need to be biased.

Heater Filaments – GDS Layer 39 (Light field): This layer defines the heater filaments. Drawn objects on this layer will remain after metal lift-off. It is recommended to use a filament width of 2 μm for the best compromise between heater power efficiency, phase tunability and robustness.

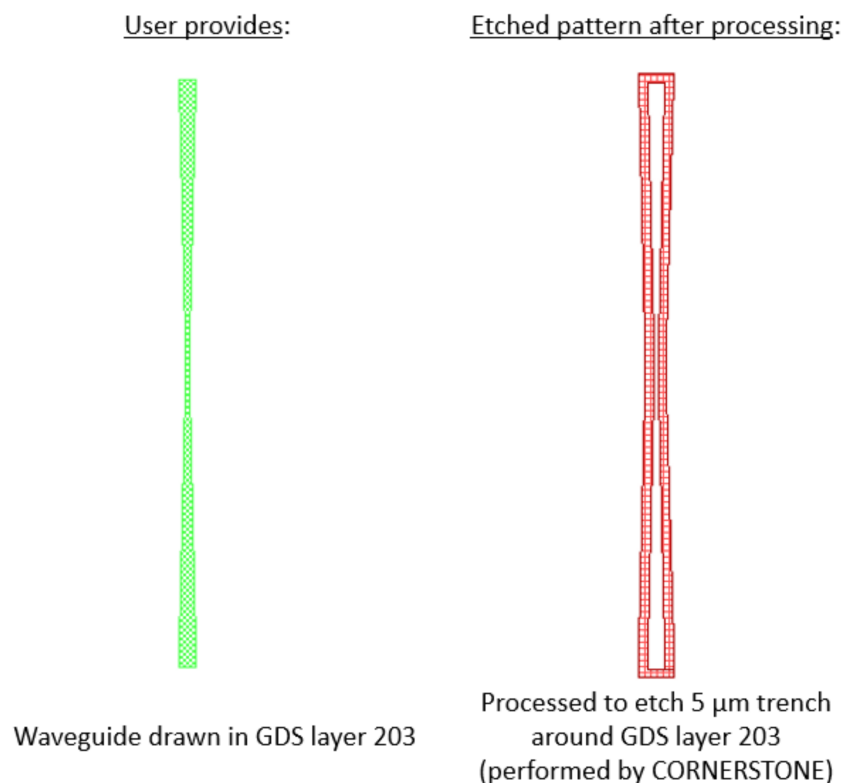


Figure 1: Description of GDS Layer 203 processing.

Heater Contact Pads – GDS Layer 41 (Light field): This layer defines the heater contact pads. Drawn objects on this layer will remain after metal lift-off. An example heater layout for a straight waveguide is included in the .gdsII template file. The contact pads can be modified according to your probe design.

Cladding opening window – GDS Layer 22: This layer defines the area for oxide cladding etching. Drawn objects in this layer will be etched. Dense arrangements of waveguide structures (gaps < 400 nm) within the opening windows are susceptible to undercuts. A rule is in place within the DRC script to provide feedback to users. Warnings resulting from this additional rule will not be considered as DRC errors and will be automatically waived.

Labels – GDS Layer 100: This layer defines text labels, which will be merged with Silicon Nitride Etch 1 layer by the CORNERSTONE team. This layer will not have any design rule checking (DRC) performed.

Information layers: These layers are purely informative and their contents will not be transferred onto the chips during fabrication.

Physical PD Area – GDS Layer 140/1: This layer shows the physical boundary of the bonded PD on the finalised chips.

PD Active Area – GDS Layer 147/1: This layer shows the active area of the photodiodes for the convenience of the user.

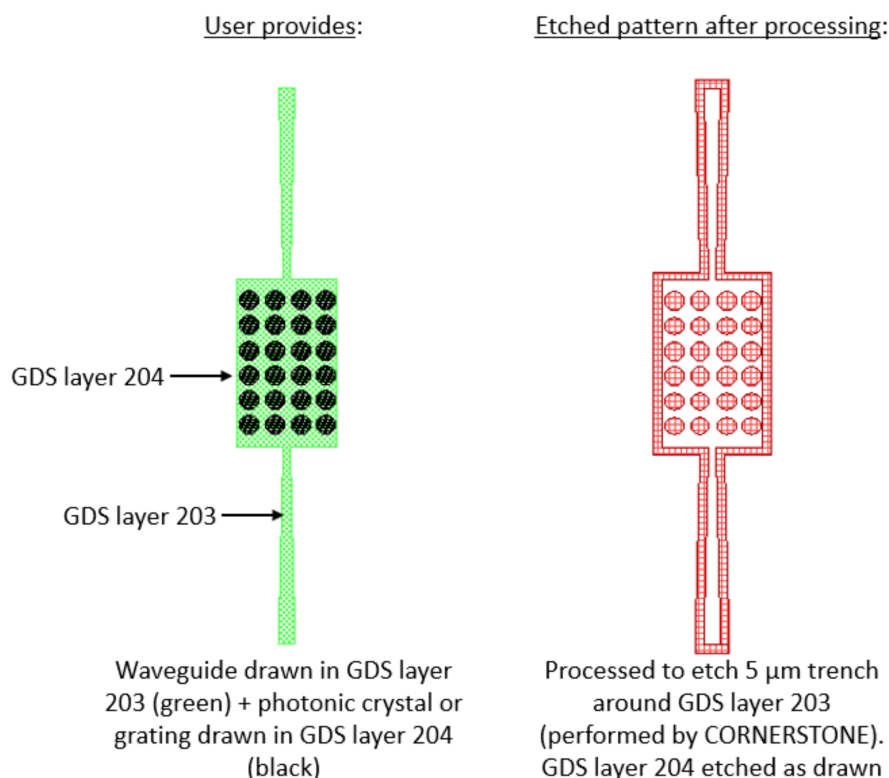


Figure 2: Example photonic crystal structure using GDS Layers 203 & 204.

PD Exclusion Zone - GDS Layer 150/1: This layer shows the exclusion zone for a single PD. Packaging DRC checks will solely include this layer.

Cell Outline – GDS Layer 99: This layer defines the design space boundaries (11.47 x 15.45 mm²).

Note: You do not need to add fabrication alignment marks to your design. Layer-to-layer alignment marks will be added by the CORNERSTONE team, placed outside the design area. Likewise, PD designs do not require any additional alignment markers.

5.3 MINIMUM FEATURE SIZES AND OTHER DESIGN RULES

- Minimum feature sizes, minimum gaps, and maximum feature widths for each GDS layer are detailed in Table 4.
- A minimum spacing between waveguides of at least 10 µm is recommended to avoid power coupling.
- An overlap of at least 2 µm between GDS layer 39 (Heater Filaments) and GDS layer 41 (Heater Contact Pads) is recommended for optimal heater performance.
- Minimum size for a cladding opening should be at least 20 x 20 µm².
- The structures on layers 140/1, 147/1 and 150/1 will not be processed and no DRC operations will be performed on them. The responsibility of appropriate photodiode placement using the information on these layers lies with the customer.

5.4 DESIGN RULES SUMMARY

A summary of the design rules and GDS layer numbers described in this section is detailed below.

Table 4: Access cost and Delivery Time

Layer Description	GDS Number	Field	Min. Feature Size	Min. Gap	Max. Feature Length
Silicon Nitride Etch 1	203	Light	250 nm	250 nm	20 μ m
			350 nm	250 nm	N/A
	204	Dark	250 nm	250 nm	20 μ m
			250 nm	350 nm	N/A
Heater Filaments	39	Light	600 nm	5 μ m	N/A
Heater Contact Pads	41	Light	2 μ m	5 μ m	N/A
Cladding Opening Window	22	Dark	20 μ m	20 μ m	N/A
Physical PD Area	140/1	N/A	N/A	N/A	N/A
PD Active Area	147/1	N/A	N/A	N/A	N/A
PD Exclusion Zone	150/1	N/A	N/A	N/A	N/A
Cell Outline	99	N/A	N/A	N/A	N/A
Labels†	100	Dark	250 nm	250 nm	N/A

*For the waveguide layer there is a maximum feature length restriction of 20 μ m when the minimum feature is 250 nm. This is because resist features that are long and thin can collapse during the development process. Resist widths of > 350 nm are stable and therefore there are no length restrictions for widths > 350 nm.

†Features drawn in the Labels layer will be merged into the Silicon Nitride Etch 1 layer by the CORNERSTONE team.

In order to help you ensure that you comply with the design rules, you can download and execute the KLayout pre-DRC script provided by CORNERSTONE on our website <https://cornerstone.sotonfab.co.uk/mpw/live-calls/> (note that the automatic DRC will

not check all of the design rules, so it remains very important to read the design rules in detail.)

MPW users will have an opportunity to attend 1-to-1 Drop-in Session to pre-review mask layouts before the submission deadline, using the [link](#) to book a 20-min session.

5.5 FILE FORMAT

Designs must be submitted in a Graphical Database System file (extension *.gdsII*) or Open Artwork System Interchange Standard (extension *.oas*) format. Ensure a manufacturing grid size of 1 nm is used, as per the CORNERSTONE GDSII Template file.

We recommend dedicated lithography editing software be used in the design of the *.gdsII* or *.oas* file.

5.6 GDSII TEMPLATE FILE

A *.gdsII* template file has been made available on our website containing the information described in this section. Ensure that all submitted designs fit within the specified area, and that only the designated GDS layer numbers are used.

6 MATERIAL PROPERTIES

The measured refractive index of the LPCVD silicon nitride layer is shown in Figure 3 below. This data is also available in tabular format on our website.

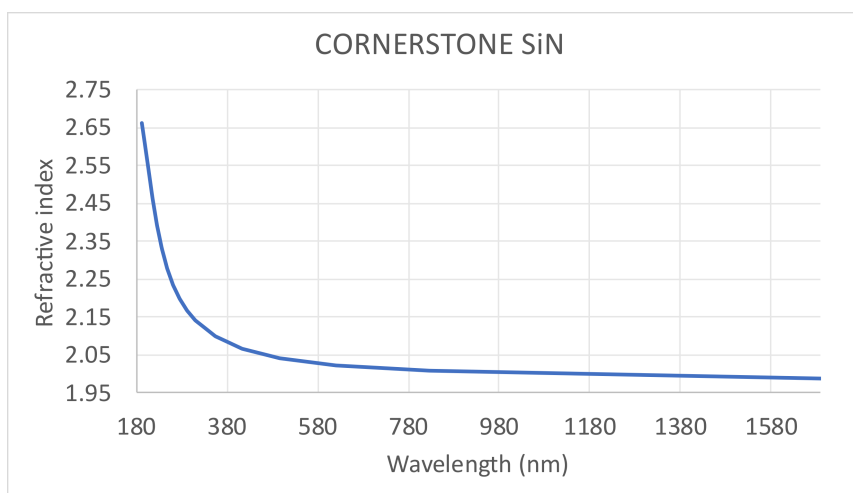


Figure 3: Silicon nitride refractive index

7 QUALITY ASSESSMENT

This fabrication run will be qualified by characterising a standard test pattern that is included on the chip (not part of the user cell). The test structures that will be checked after fabrication are reported in Table 5, together with the values that are targeted by the CORNERSTONE platform.

Table 5: Quality assessment parameters

Test Structure	Parameter	Value
Straight single mode strip waveguide	Propagation loss	< 0.6 dB/cm for TE mode in C-band
MZI integrated with the PDK heater	Phase shift efficiency	< 175 mW/ π phase shift
Flip-chip bonded photodiode	Responsivity	> 0.5 A/W @ $\lambda = 1550$ nm

8 MASK SUBMISSION PROCEDURE

In order to be eligible to submit a design you must first sign-up to this call using the online form found using the link below. This is in order to enable us to prepare the necessary paperwork and plan the fabrication process effectively. The sign-up deadline is found at the top of this document.

www.cornerstone.sotonfab.co.uk/home/mpw-sign-up-form

Under no circumstances will we accept any design submissions for which we have not received a sign-up form.

After completing the sign-up form, when you are ready to submit your mask design on or before the mask submission deadline listed at the top of this document, follow the link below to the CORNERSTONE website mask submission page:

www.cornerstone.sotonfab.co.uk/gds-file-upload

A purchase order (PO) must be uploaded to this form to pay the access fee. Purchase orders will not be accepted via email.

You must also upload your design file to the submission form. Ensure that the top cell in your design file is titled 'Cell0_[Name of Institution]'.

For information about setting up CORNERSTONE as a supplier to your institution, or if you encounter any problems with the online forms, please contact cornerstone@soton.ac.uk

9 MASK PROCESSING PERFORMED BY CORNERSTONE

Upon receipt of your .gdsII file, the CORNERSTONE team will perform the following mask processing steps in order to produce the final mask, based on the descriptions provided in Section 5.2.

Silicon Nitride Etch 1 GDS 203 (Light Field) – waveguides & GDS Layer 204 (Dark field) – gratings:

1. Grow Waveguide layer (GDS layer 203) by 5 μm in all directions.
2. Subtract the Waveguide layer (GDS layer 203) from the output of (1) to produce the etch trenches around the drawn waveguides.
3. Merge the output of (2) with the dark field Silicon Nitride Etch layer (GDS layer 204) and the Labels layer (GDS layer 100).

10 TECHNICAL SUPPORT

If you have any questions relating to the fabrication process or design rules, please contact the CORNERSTONE team (cornerstone@soton.ac.uk).

11 DEVICE DELIVERY

A total of 10 replica cells will be delivered to each user. The delivery time schedule can be found in Table 1.

12 FEEDBACK

Feedback is essential to the CORNERSTONE team. It is required to ensure a continuous improvement to the quality of our services. It is also evidence on the user satisfaction, and a measure to what extent we were able to meet user requirements. Therefore, we kindly ask our users to provide feedback to us, including device performance data, SEM images, future interests for the CORNERSTONE project etc. A feedback form will be sent to you along with your chips.

Alternatively, email cornerstone@soton.ac.uk with your comments.

13 PUBLICATIONS

If you are benefitting from subsidised access via the C-PIC funding, please include the following statement in the “Funding” section of any publications:

“The chip fabrication for this research was funded by the Engineering and Physical Sciences Research Council (EPSRC) C-PIC (EP/Z531066/1) project.”

This is important to us to be able to demonstrate impact from the funding. If you are a paying user, we kindly ask that you include CORNERSTONE in the “**Acknowledgments**” section of any publications that result from the chips you receive from CORNERSTONE.